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MS-7820 ATX Ver: 1.0

Intel -ShakeBay plamform

CPU:

INTEL-Haswell LGA1150

CPU DISPLAY

DVI(portC)

System Chipset:

INTEL-LYNX

OnBoard Chipset:

HD Audio Codec:ALC887

LAN-RTL8111G Co-lay 8106G

SIO:Nuvoton NCT6779

Main Memory:

DDRIII (1066/1333/1600MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

PCI Slot * 3

PWM:

VRD12 - ISL95812

Other:

SATA(SATA2-300MB/s) *2

SATA(SATA3-500MB/s) *2/4

REAL USB2.0 *4

FRONT USB2.0 *4

REAL USB3.0 *2

FRONT USB3.0 *2/4

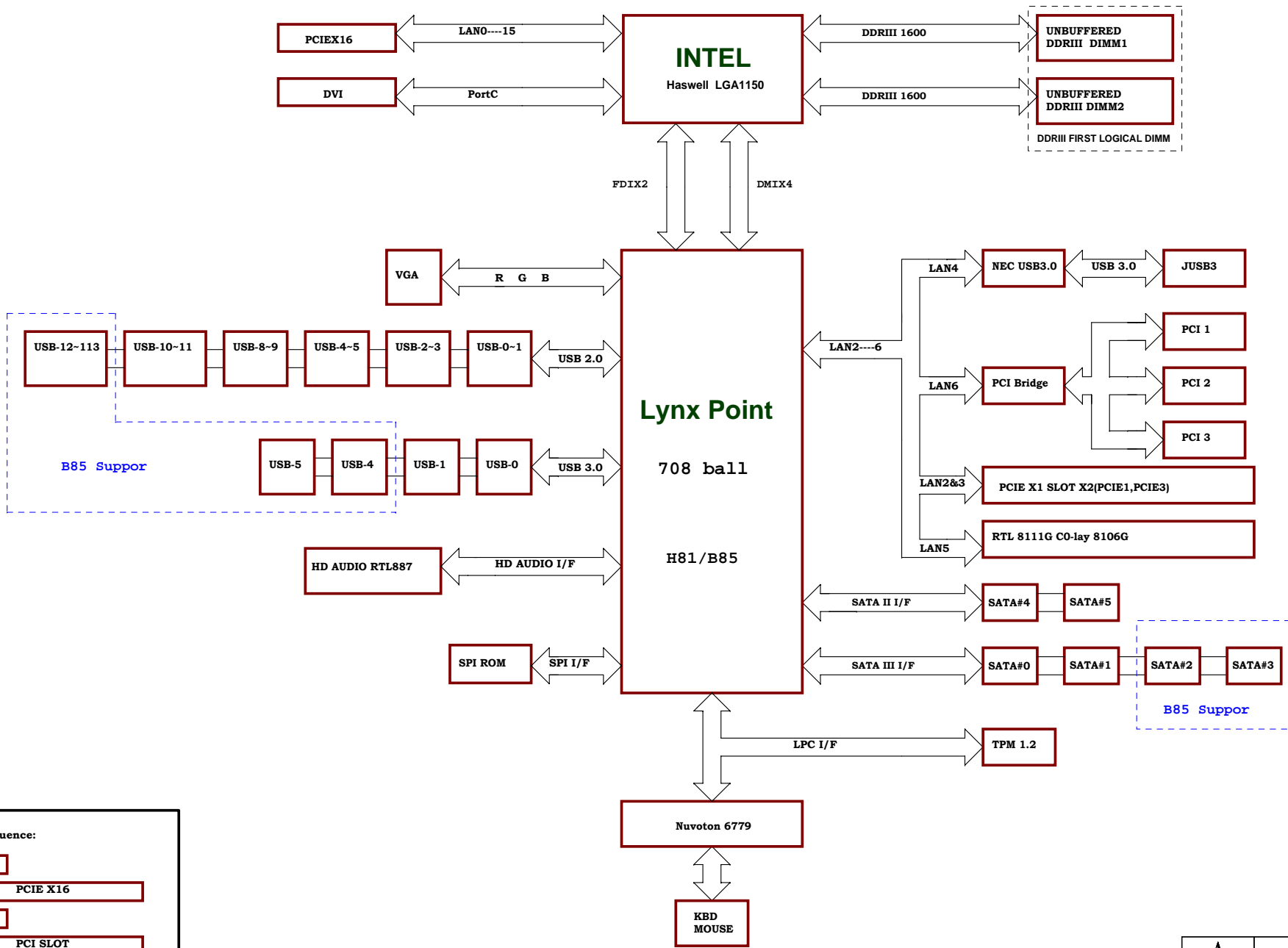


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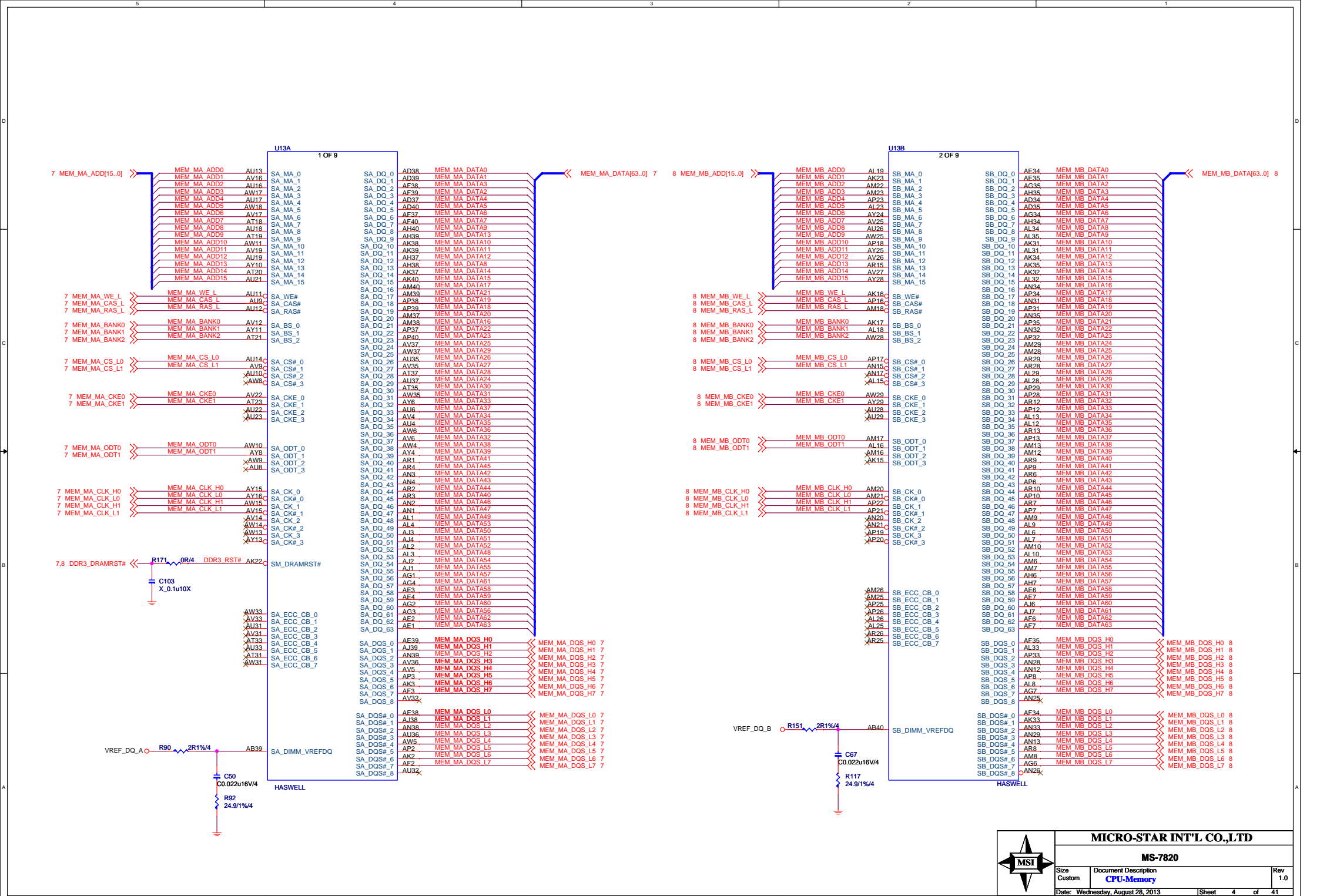
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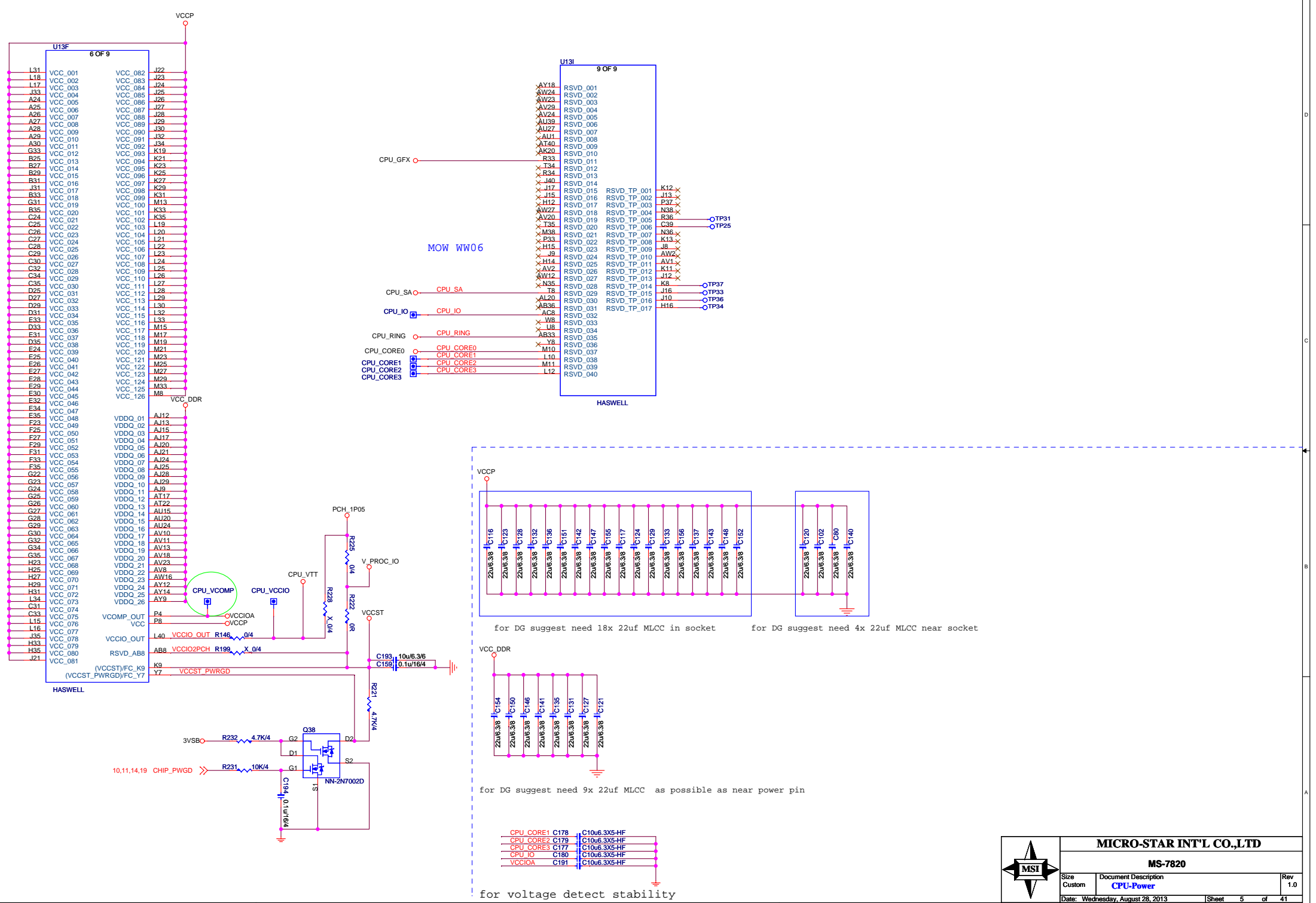
MS-7820-0A Block Diagram



Slot Sequence:

PCIE X1
PCIE X16
PCIE X1
PCI SLOT
PCI SLOT
PCI SLOT





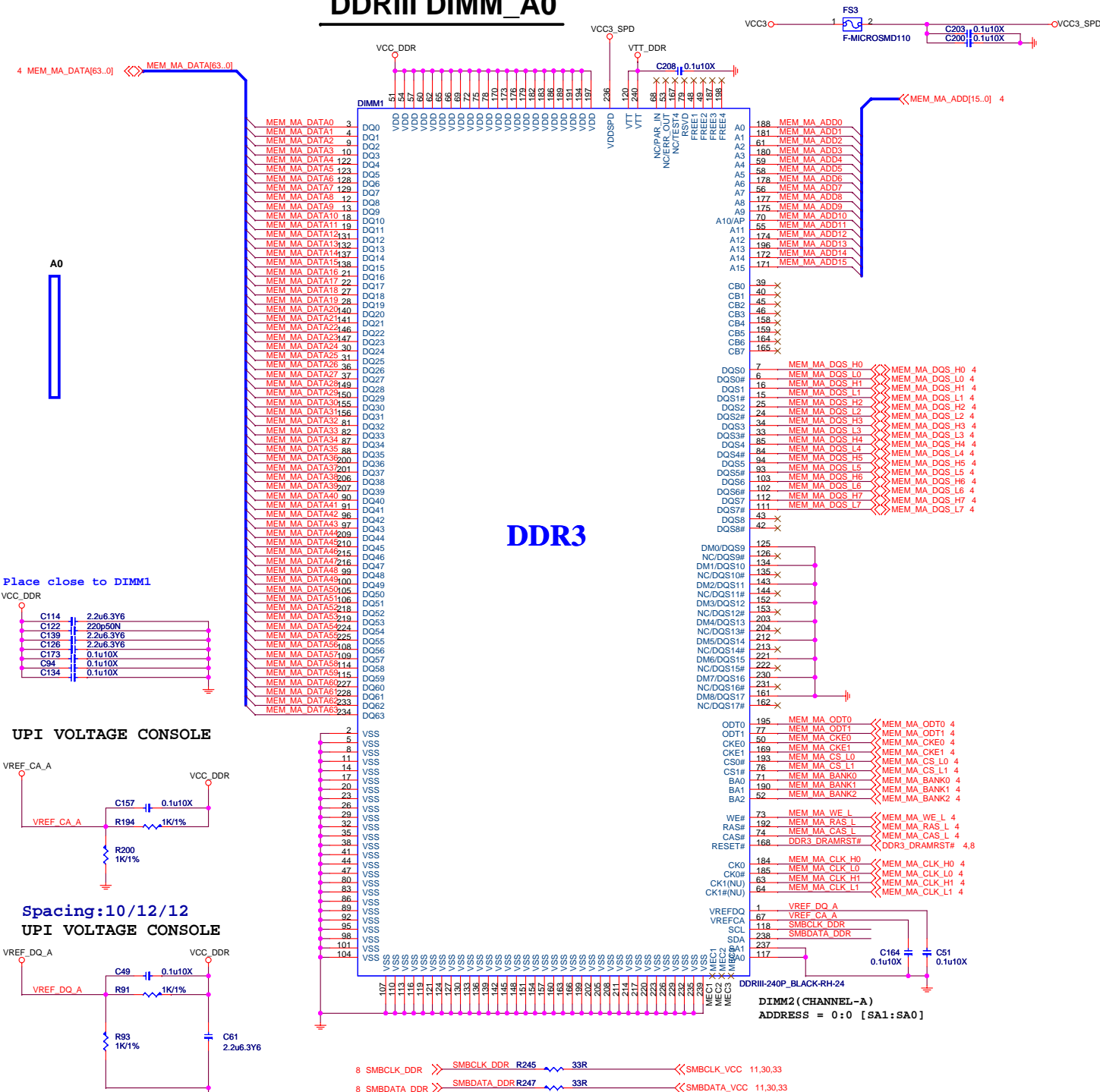
for DG suggest need 18x 22uf MLCC in socket

for DG suggest need 4x 22uf MLCC near socket

for DG suggest need 9x 22uf MLCC as possible as near power pin

for voltage detect stability

DDRIII DIMM_A0



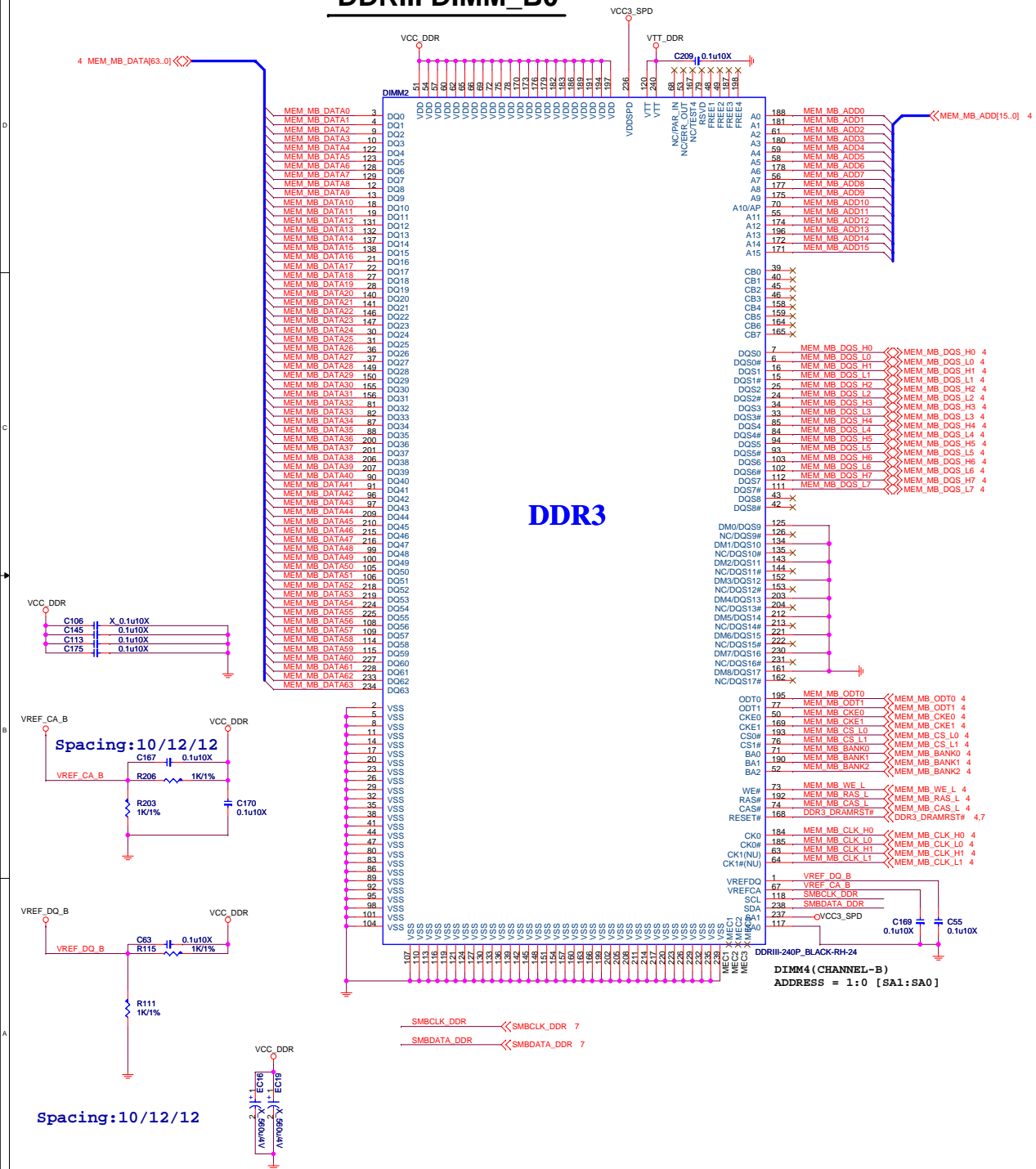
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MS-7820

Size Custom	Document Description DDR3 Chanel-A DIMM1	Rev 1.0
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DDRIII DIMM_B0

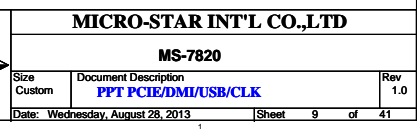
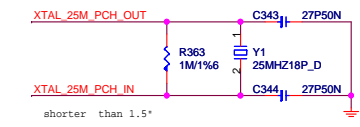
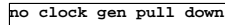


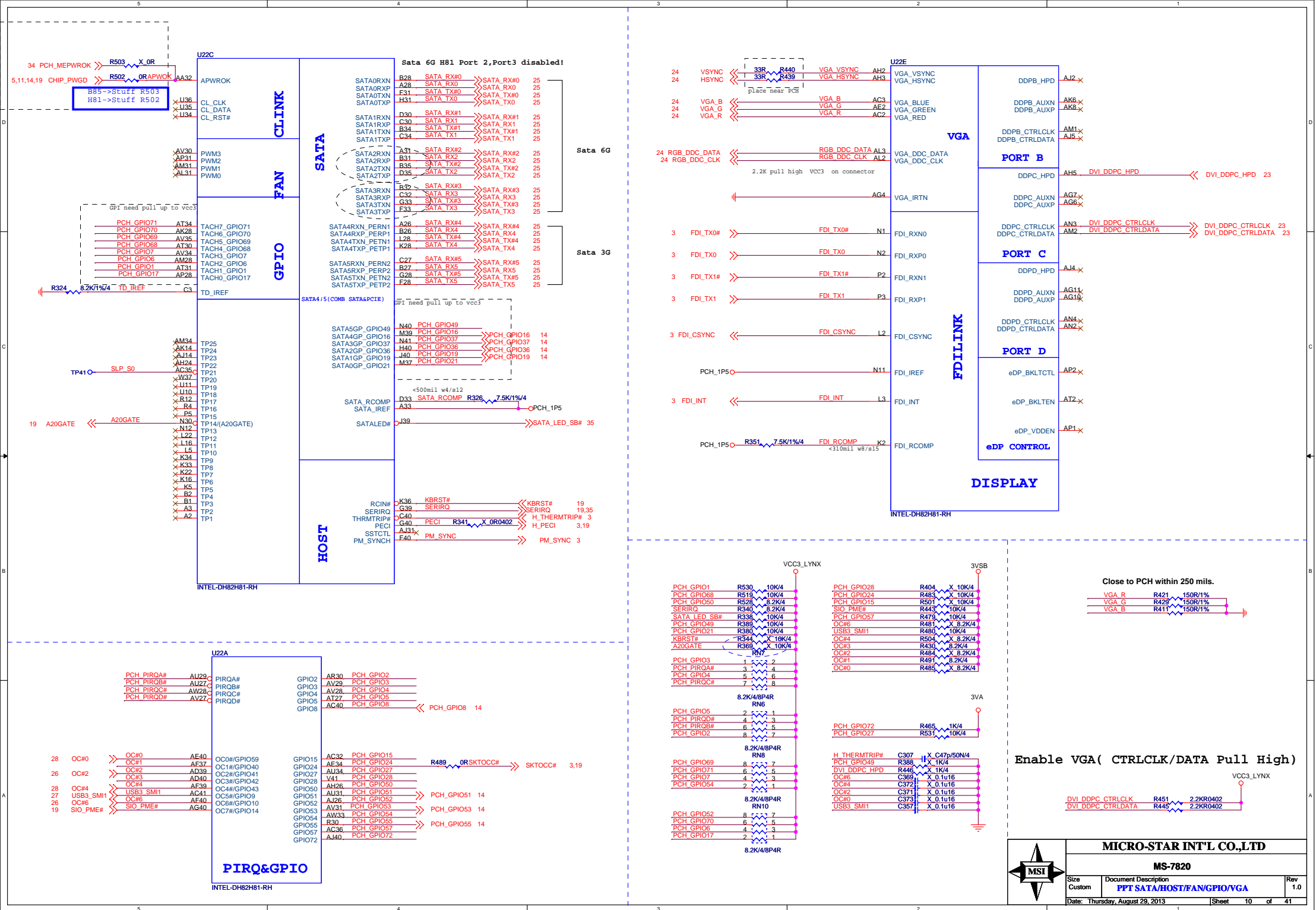
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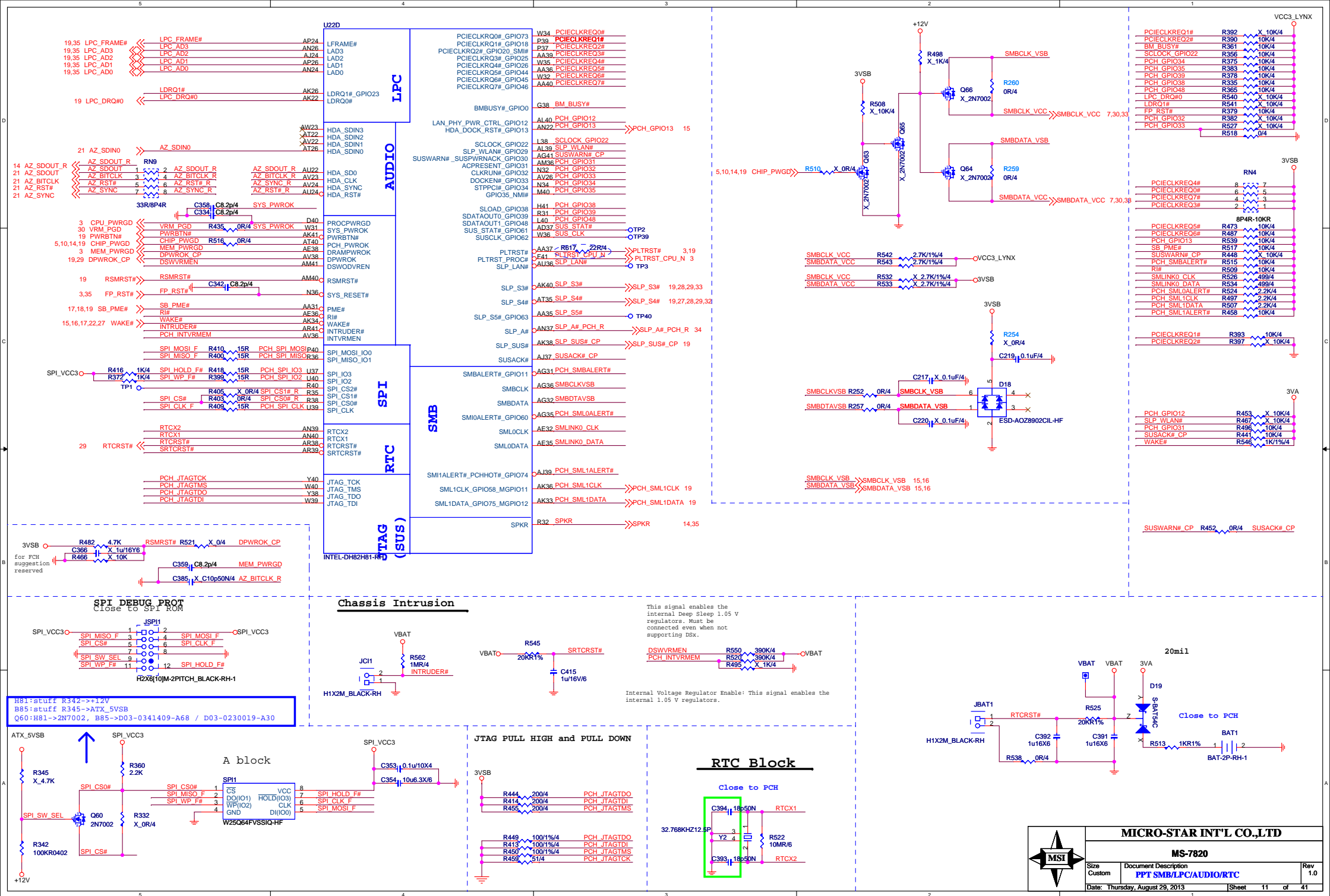
MS-7820

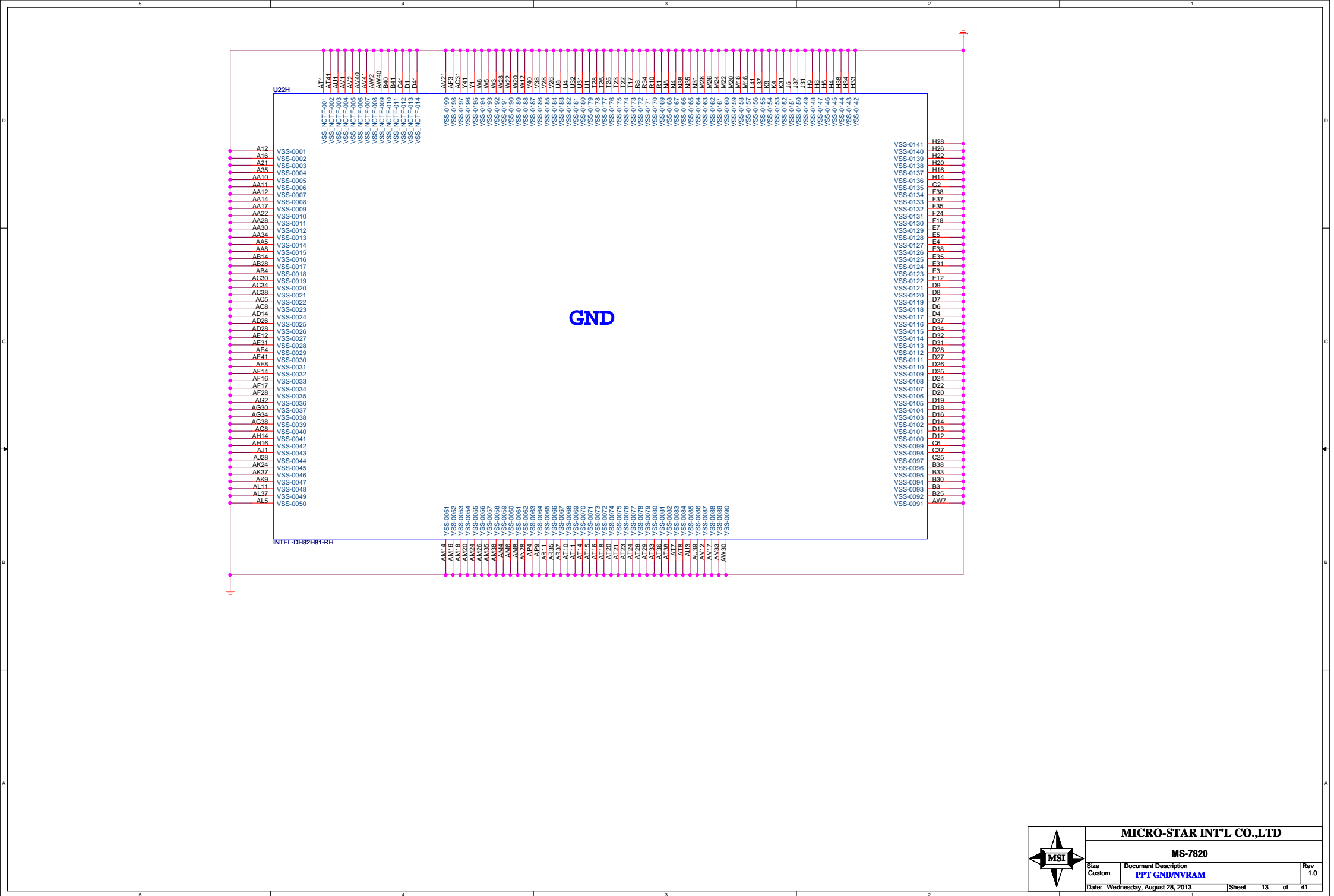
Size Custom	Document Description DDR III B DIMM 1	Rev 1.0
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```
H81 PCIE Port7,Port8 disabled!
```

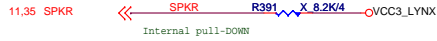






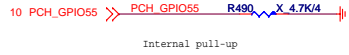


11,35 SPKR <<—SPKR R391 X 8.2K/4 VCC3_LYNX
Internal pull-DOWN

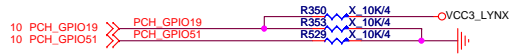


10 PCH_GPIO55 >> PCH_GPIO55 R490 X 4.7K/4

Internal pull-up



Default



10 PCH_GPIO53 >> PCH_GPIO53 R494 X 1K/4

Leave NC. Internal pull down.



10 PCH_GPIO8

PCH GPIO8

Internal pull-up

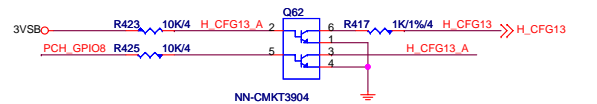
R432 X 1K/1%/4

R422 1K/1%/4

R431 1K/4

VCC3_LYNX

3VSB



10 PCH_GPIO36 >> PCH_GPIO36

R337 X 10K/4

R336 X 10K/4

VCC3_LYNX



10 PCH_GPIO16

PCH_GPIO16

R371 10K/4

R374 X 10K/4

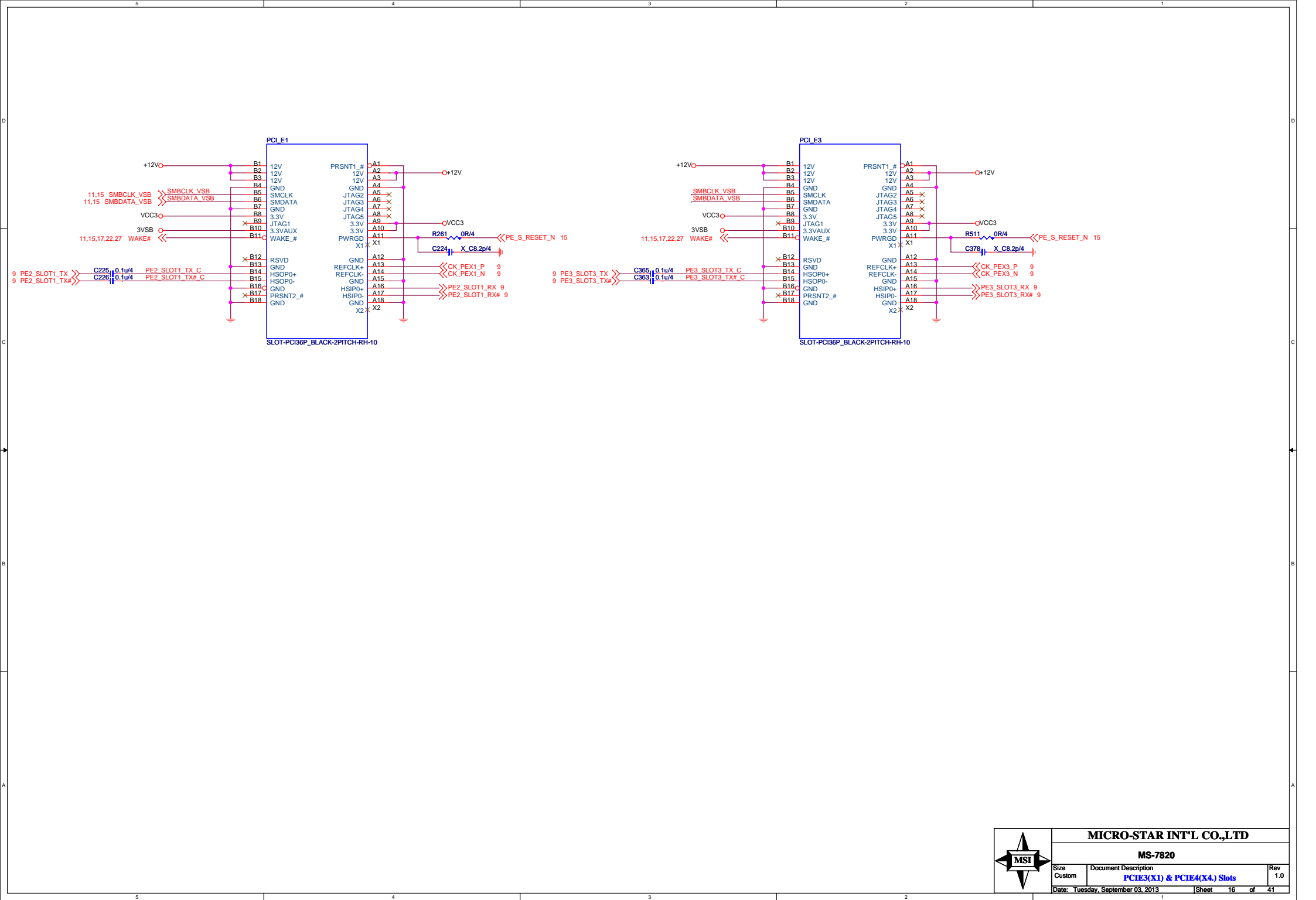
VCC3_LYNX

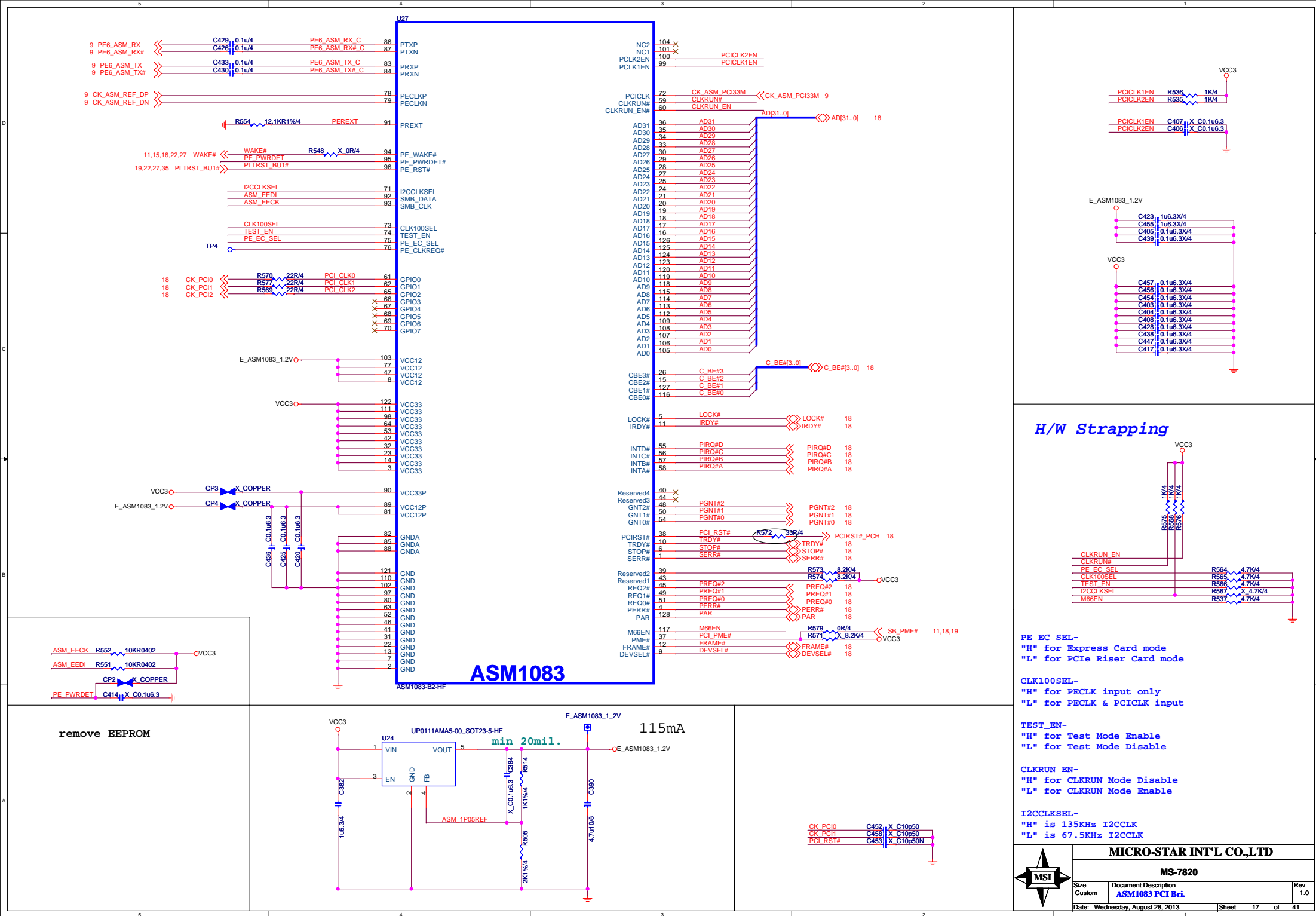
H1X2M-2PITCH

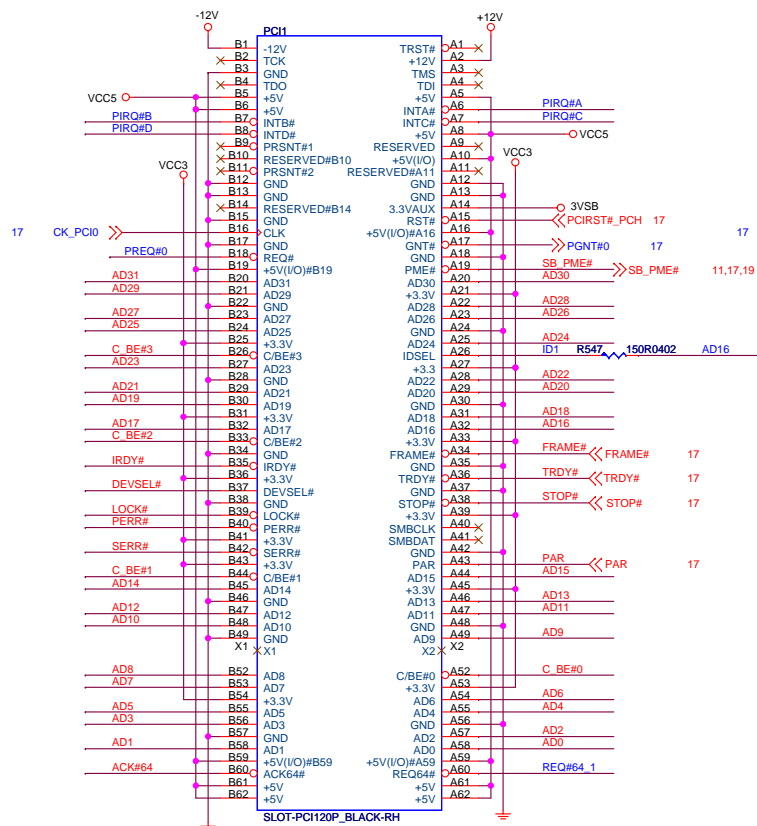
CHIP_PWGD 5,10,11,19



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MS-7820			
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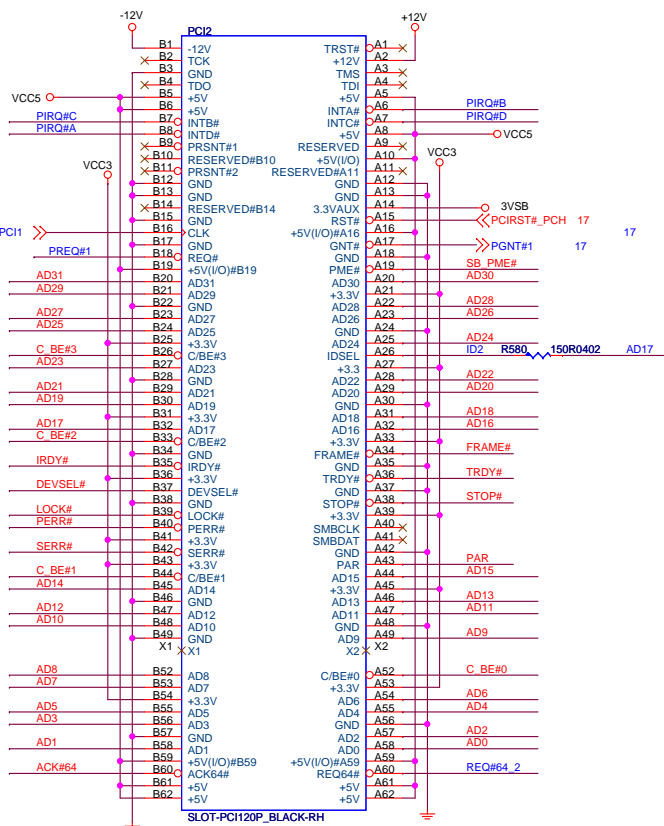
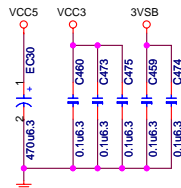






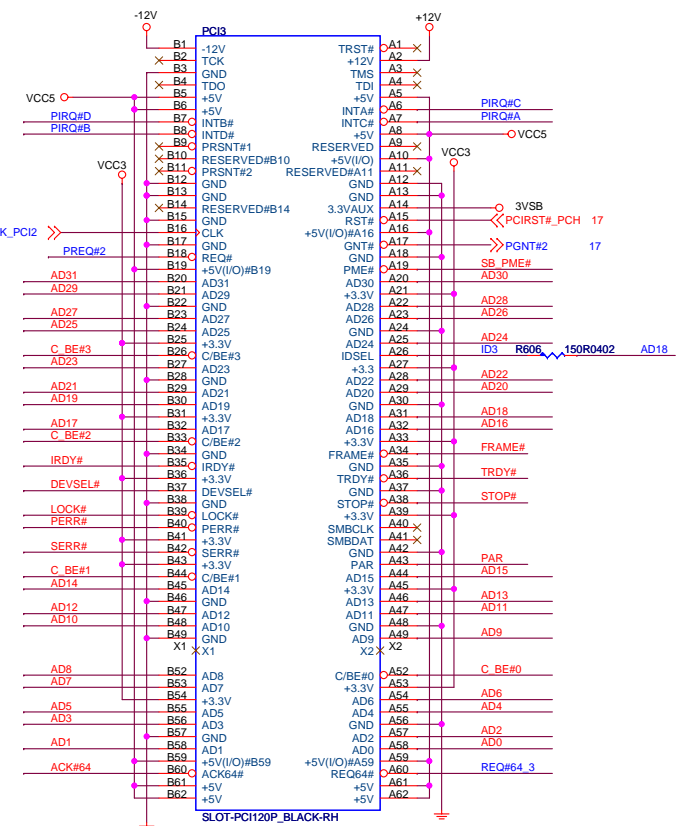
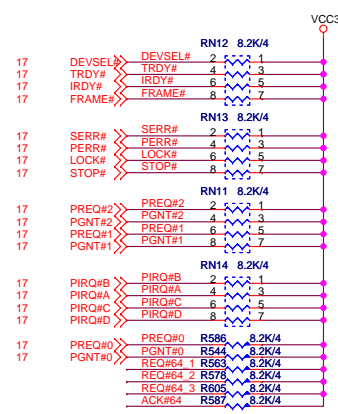
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

AD[31..0] <<> AD[31..0] 17
 C_BE#[3..0] <<> C_BE#[3..0] 17

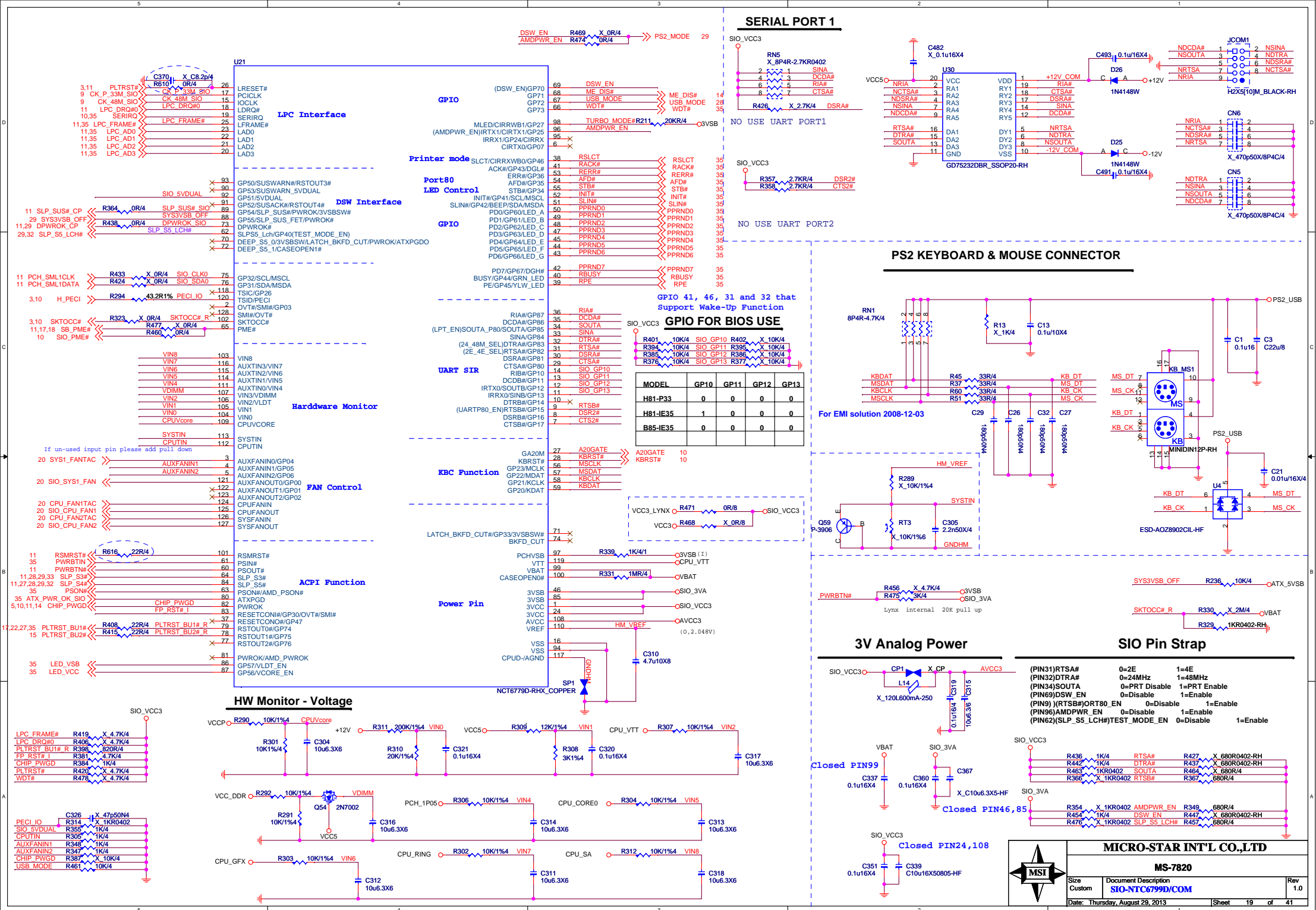


IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS

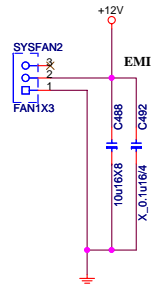


IDSEL = AD18
MASTER = PREQ#2
PIRQ#C

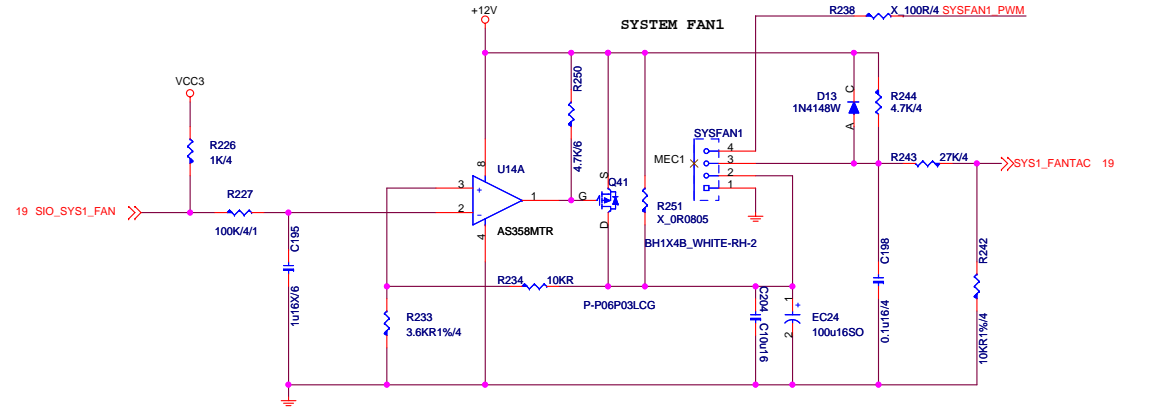
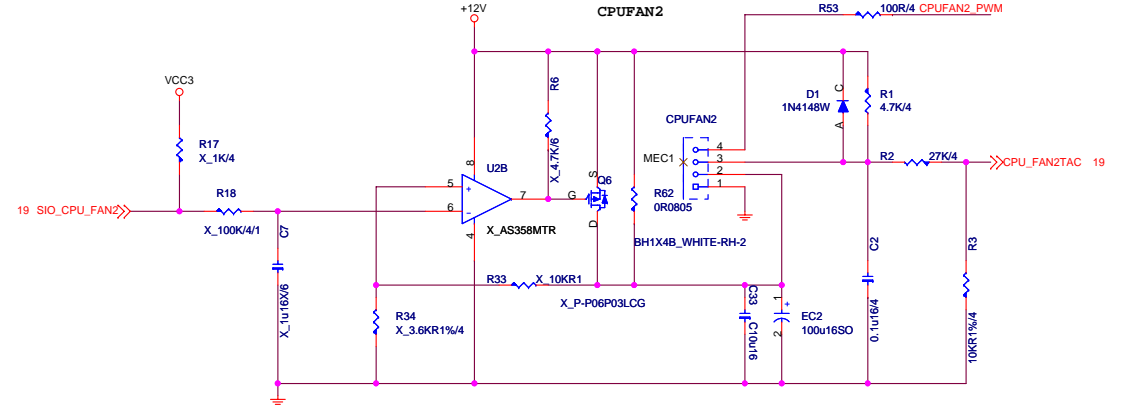
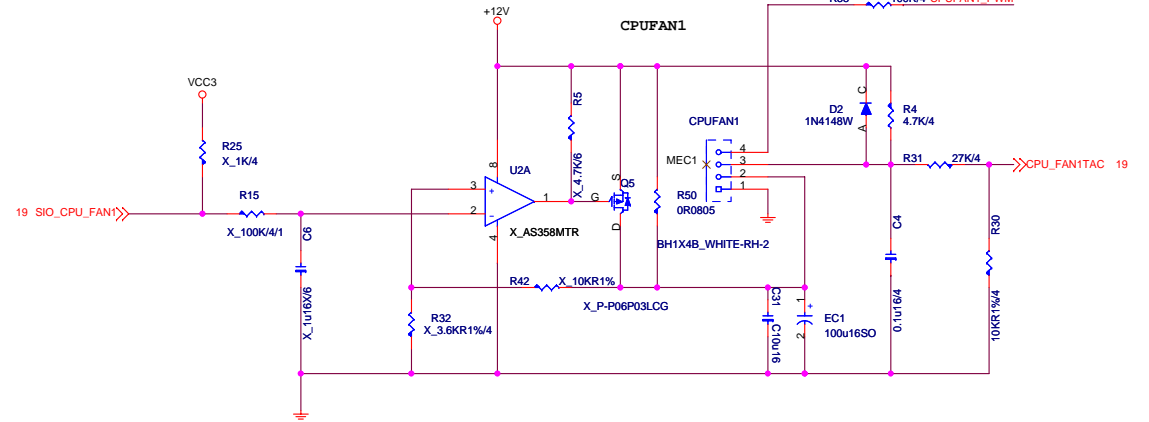
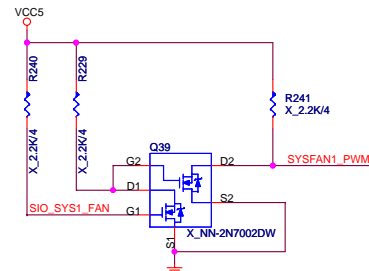
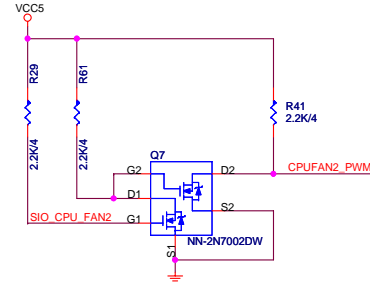
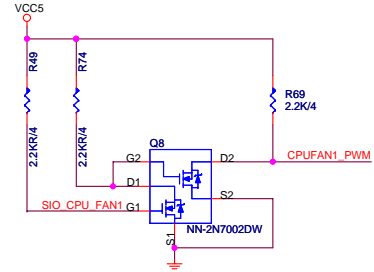
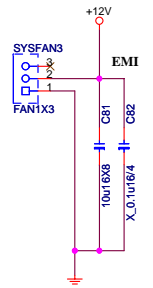


FAN-COUNTROL CIRCUIT

SYSTEM FAN2



SYSTEM FAN3

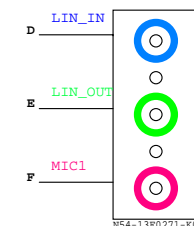
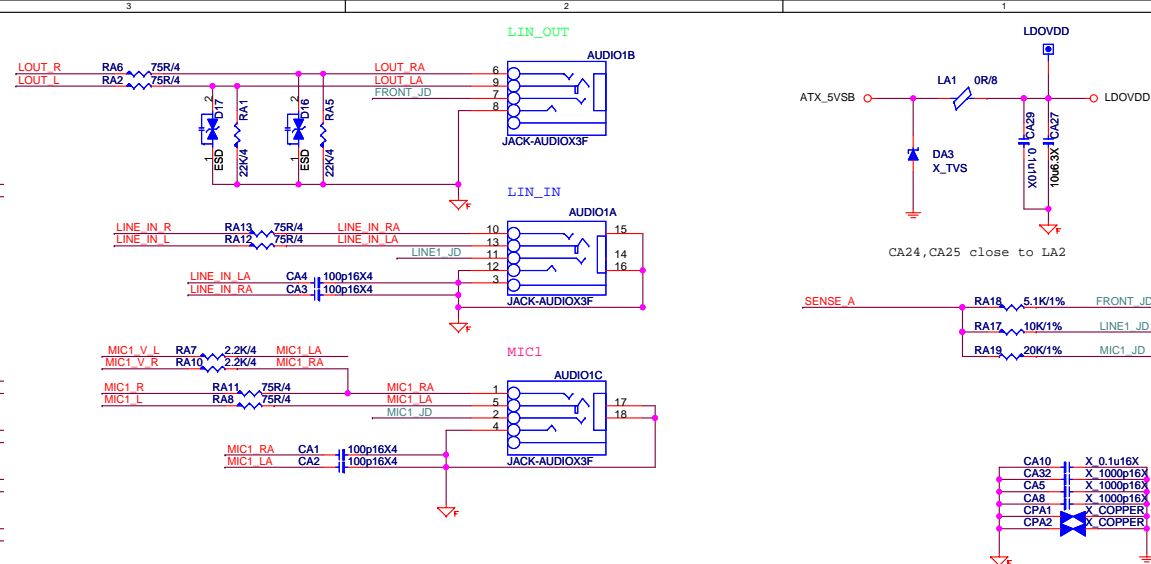
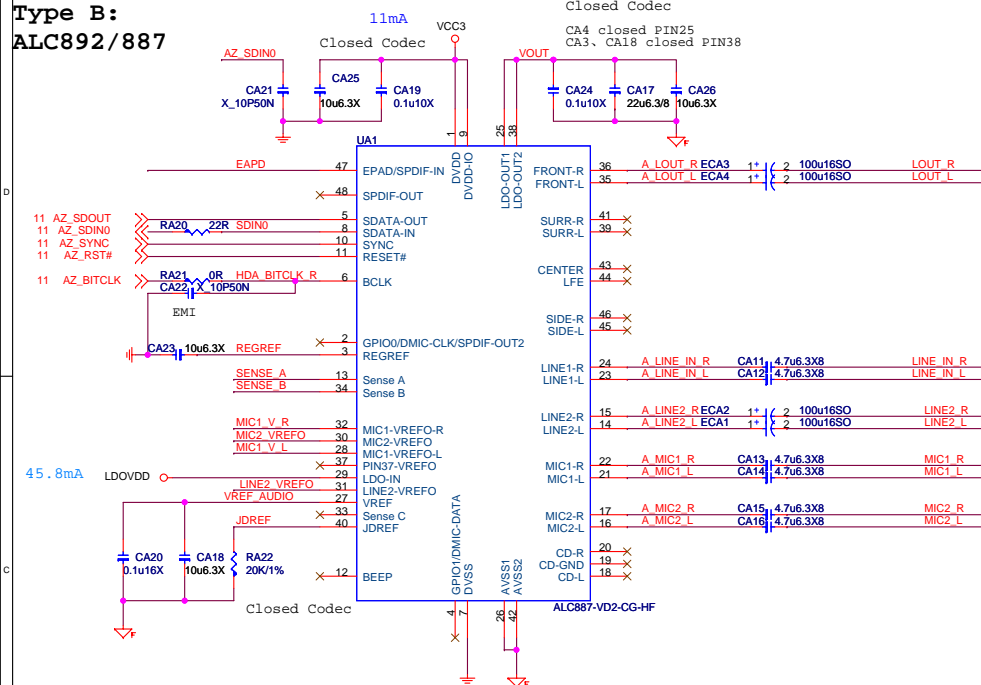


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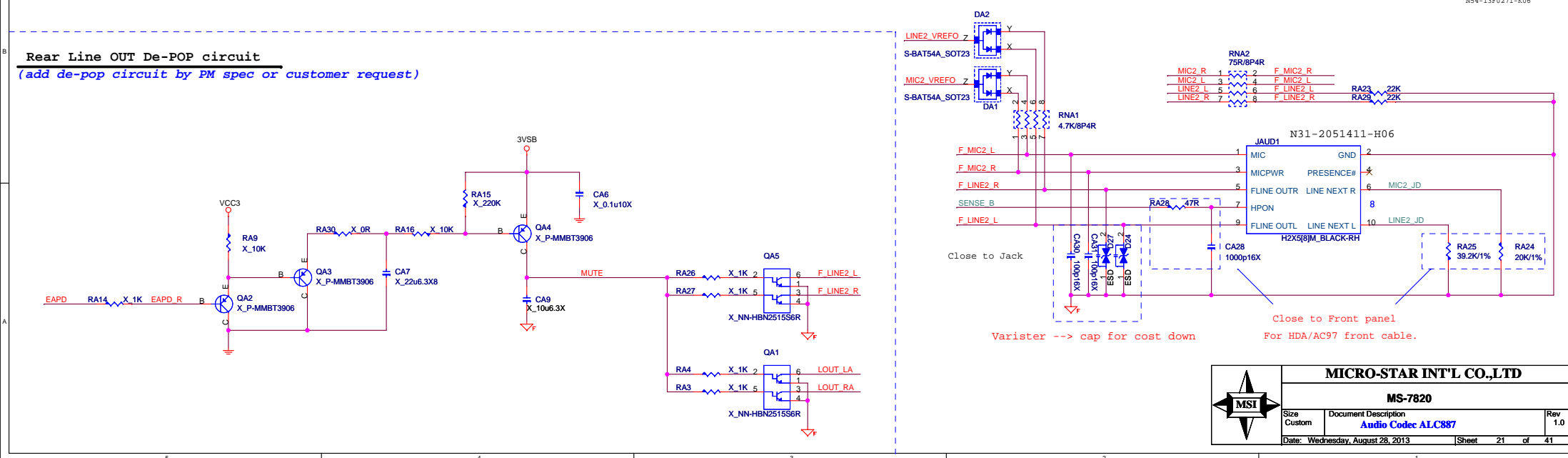
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ALC892/887



Rear Line OUT De-POP circuit

(add de-pop circuit by PM spec or customer request)



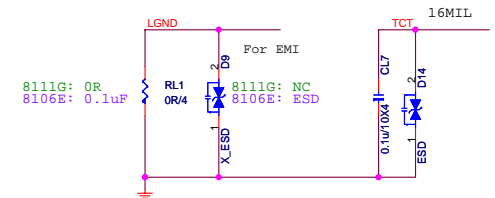
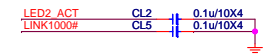
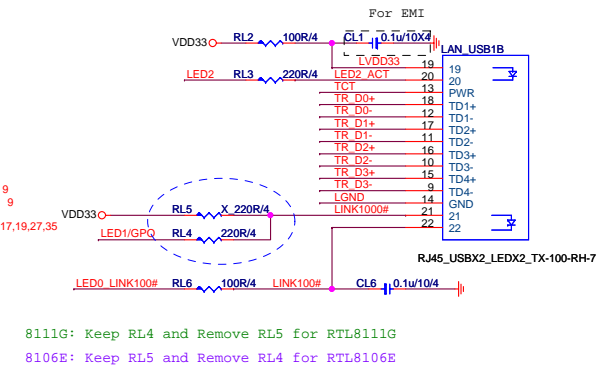
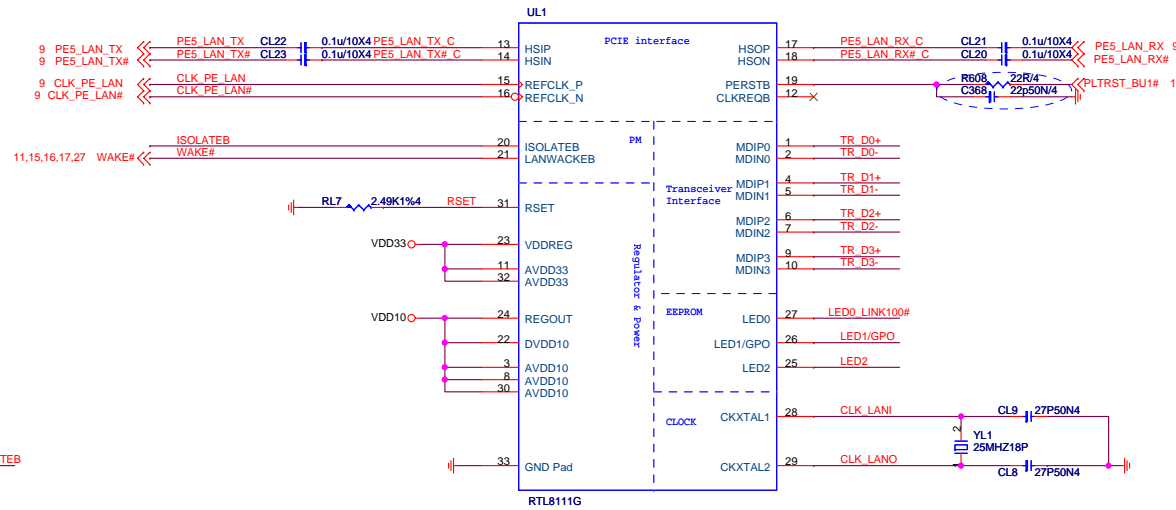
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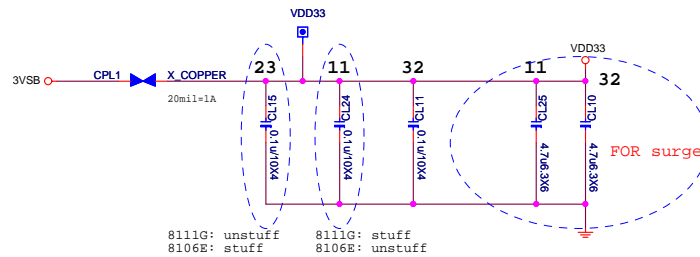
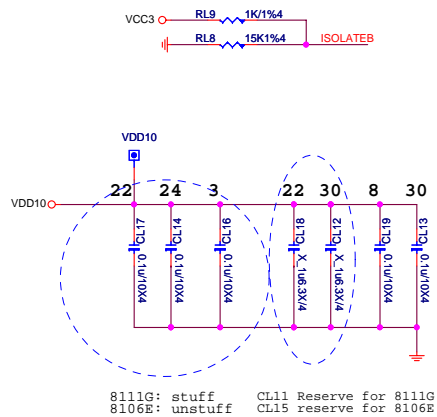
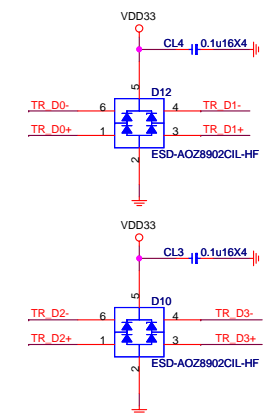
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RTL8106E 10/100M LAN

LAN Connector



Reserve ESD Protect



8106E POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	15/94	49.5/310.2
100 M Idle/TxRx	52/105	171.6/346.5
S0 ALDPS	4	13.2

8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591.8/804.9
ALDPS	6.41	21.15



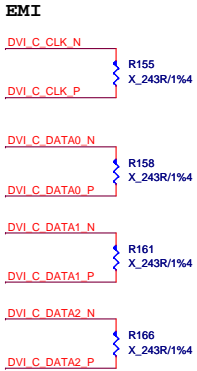
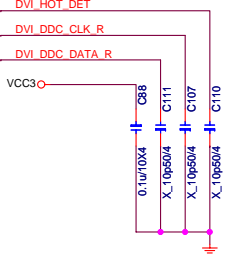
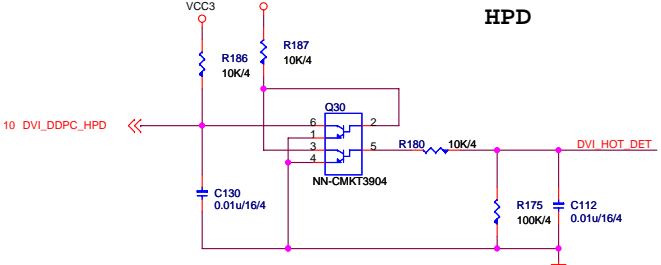
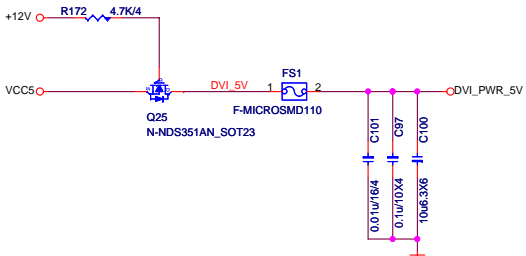
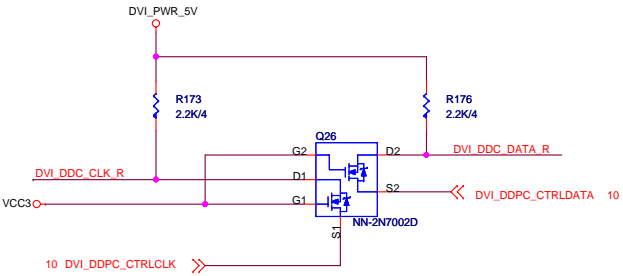
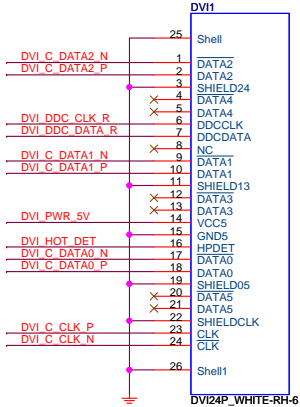
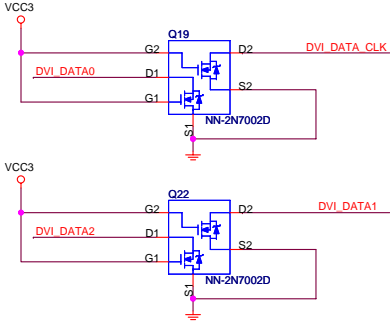
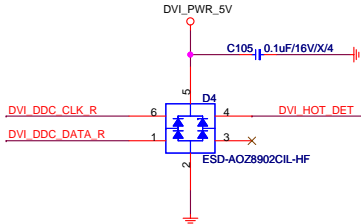
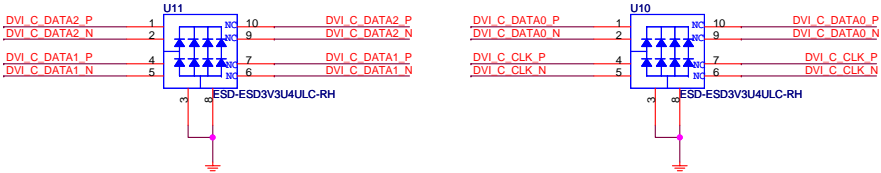
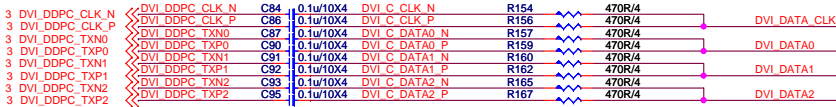
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DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	



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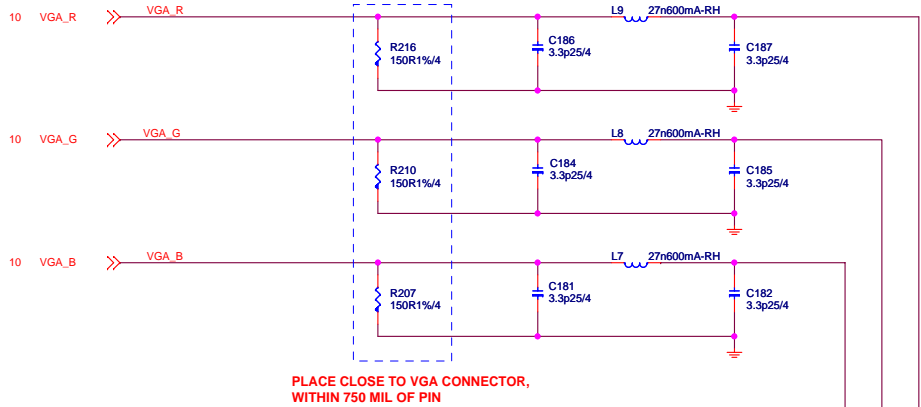
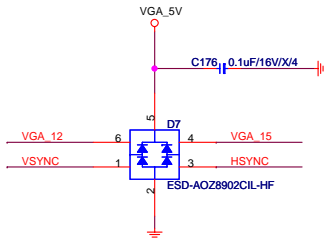
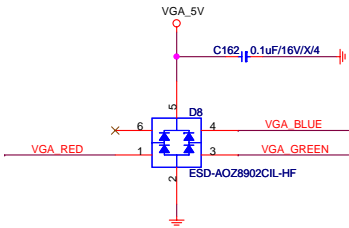
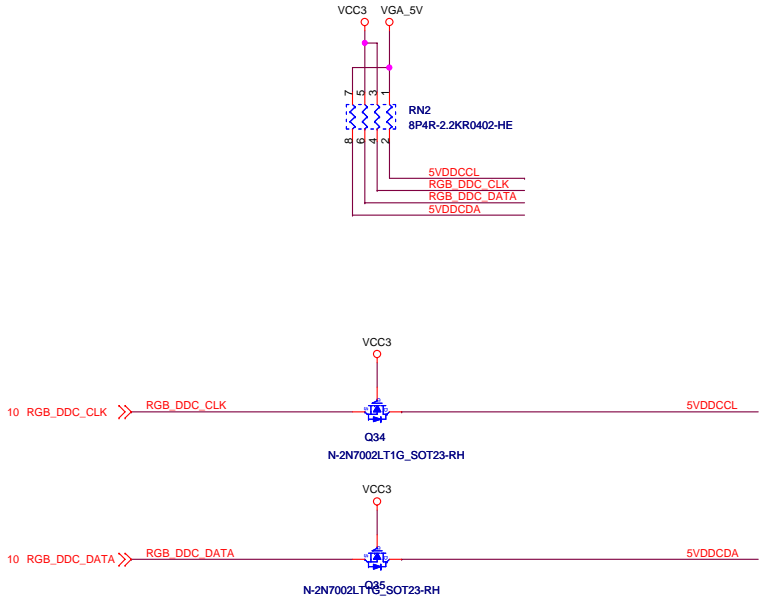
MS-7820

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Custom	DVI Connector	1.0
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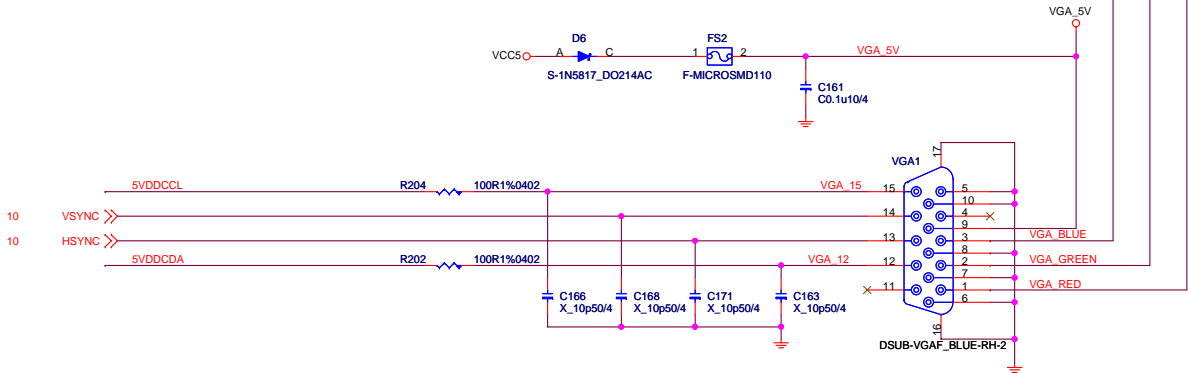
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

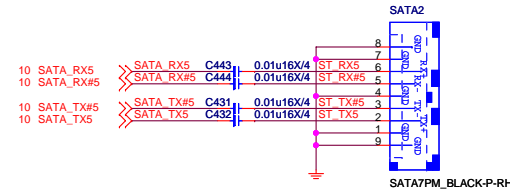
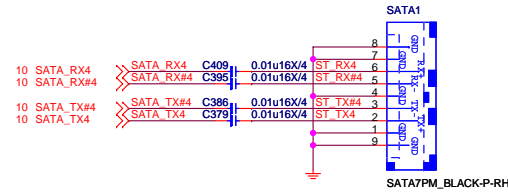
Levelshift



PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN

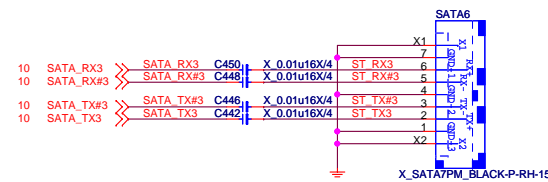
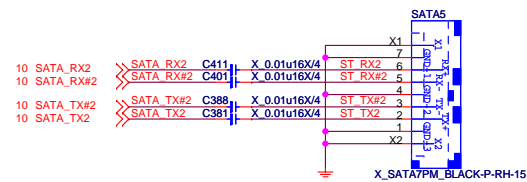
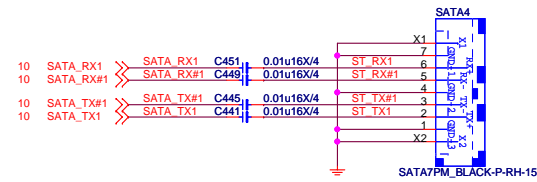
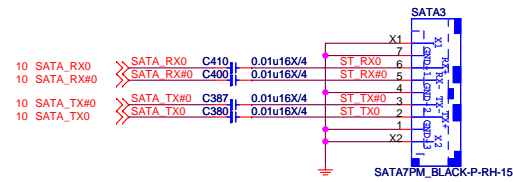


SATA 3G PORT 4,5

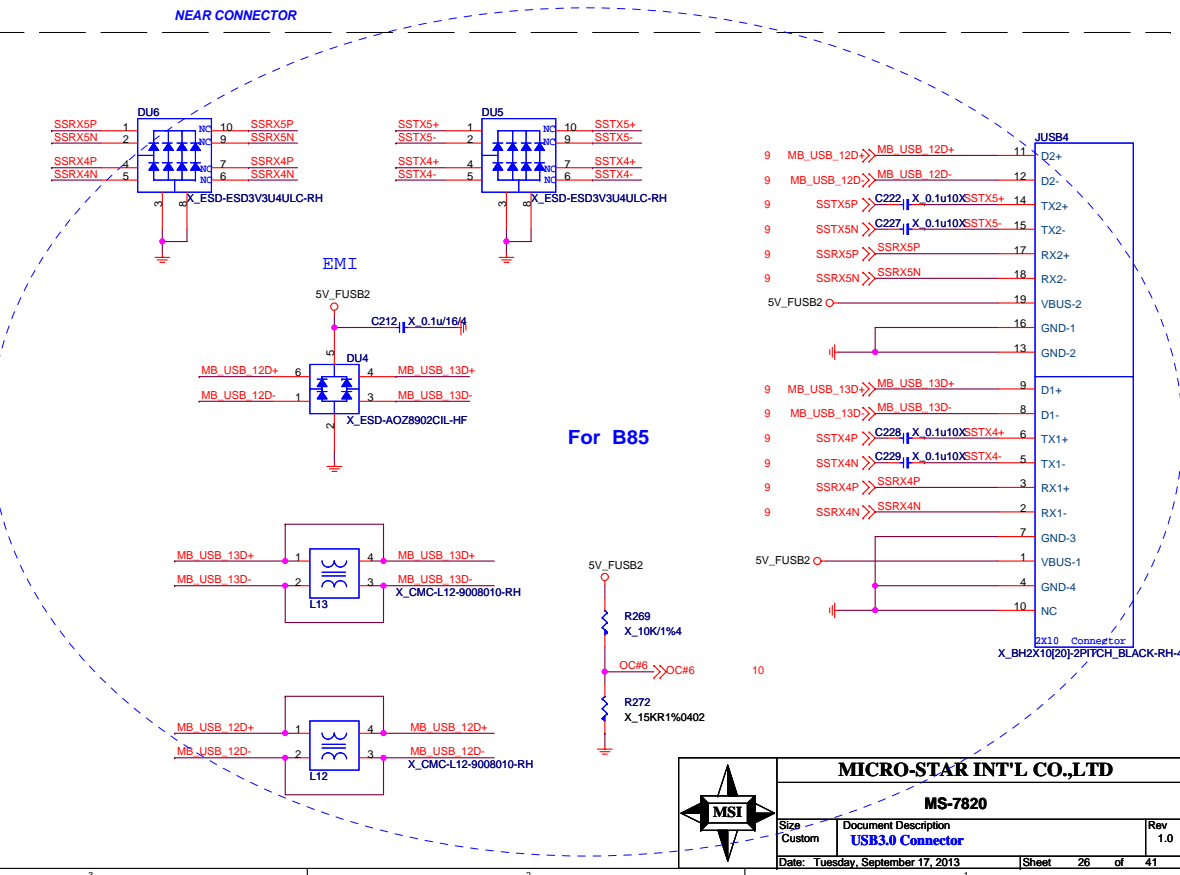
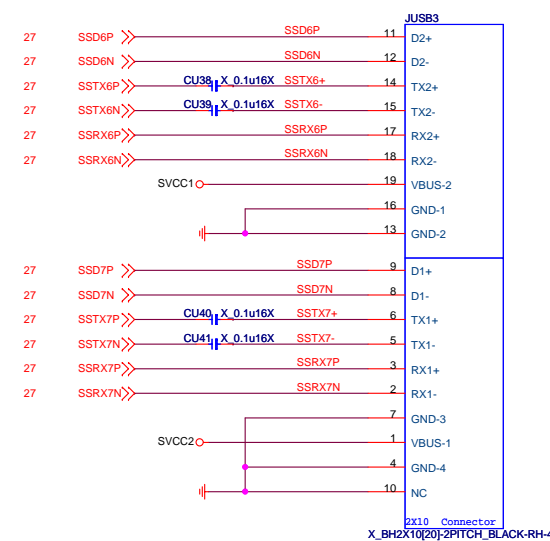
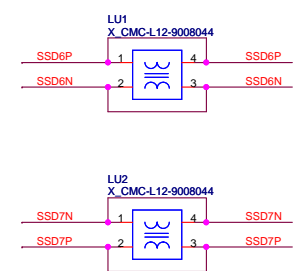
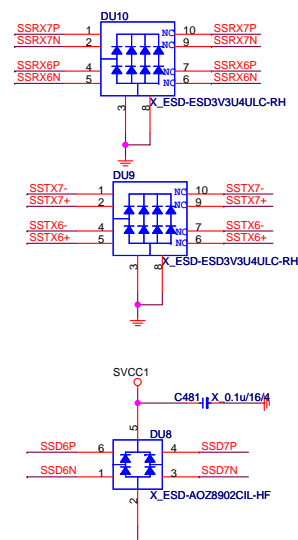
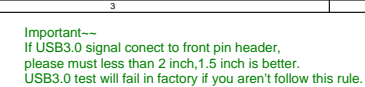
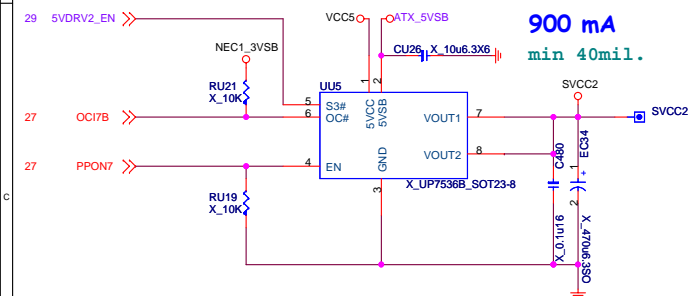


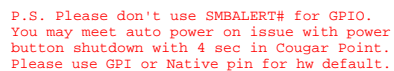
SATA 6G PORT 0,1

3.0 white



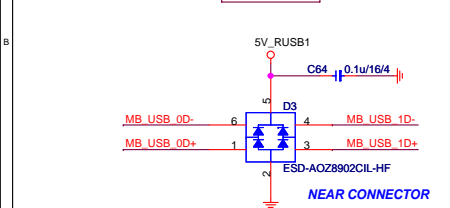
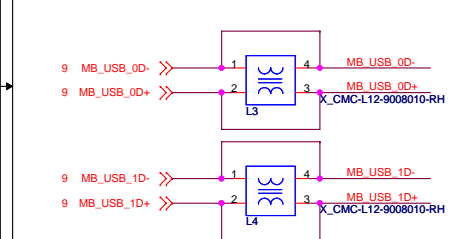
For B85



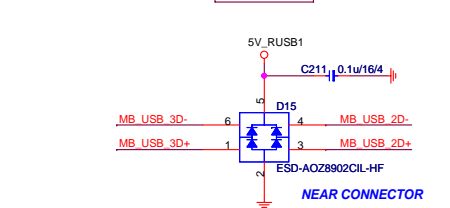
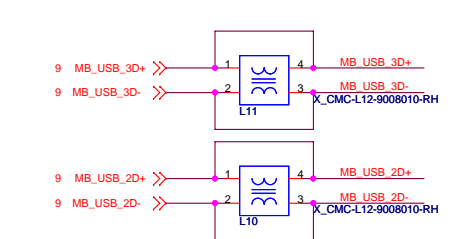


MICRO-STAR INT'L CO.,LTD			
MS-7820			
Size Custom	Document Description Renesas PD720202 USB3.0 2PORT		Rev 1.0
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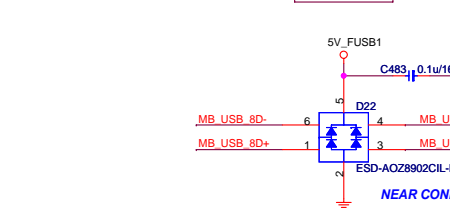
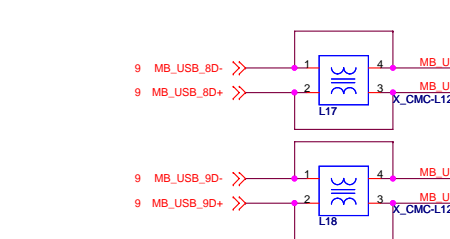
FRONT USB PORT2,3



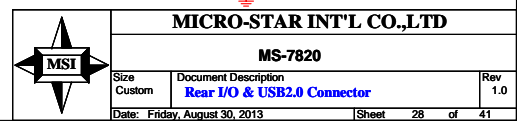
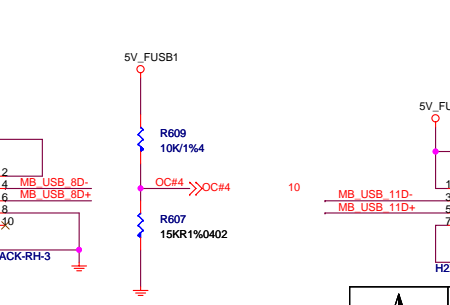
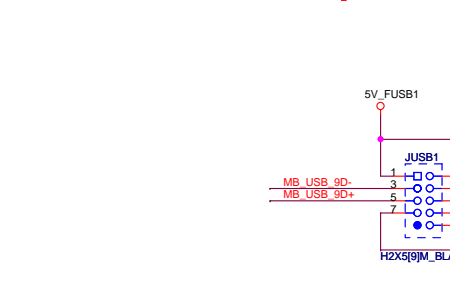
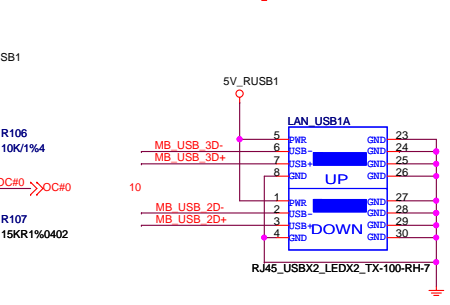
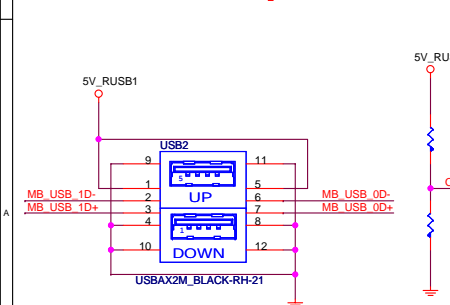
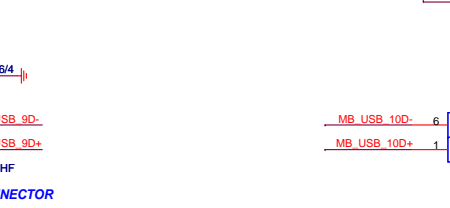
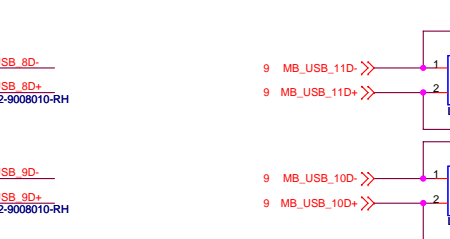
FRONT USB PORT4,5(With Lan)



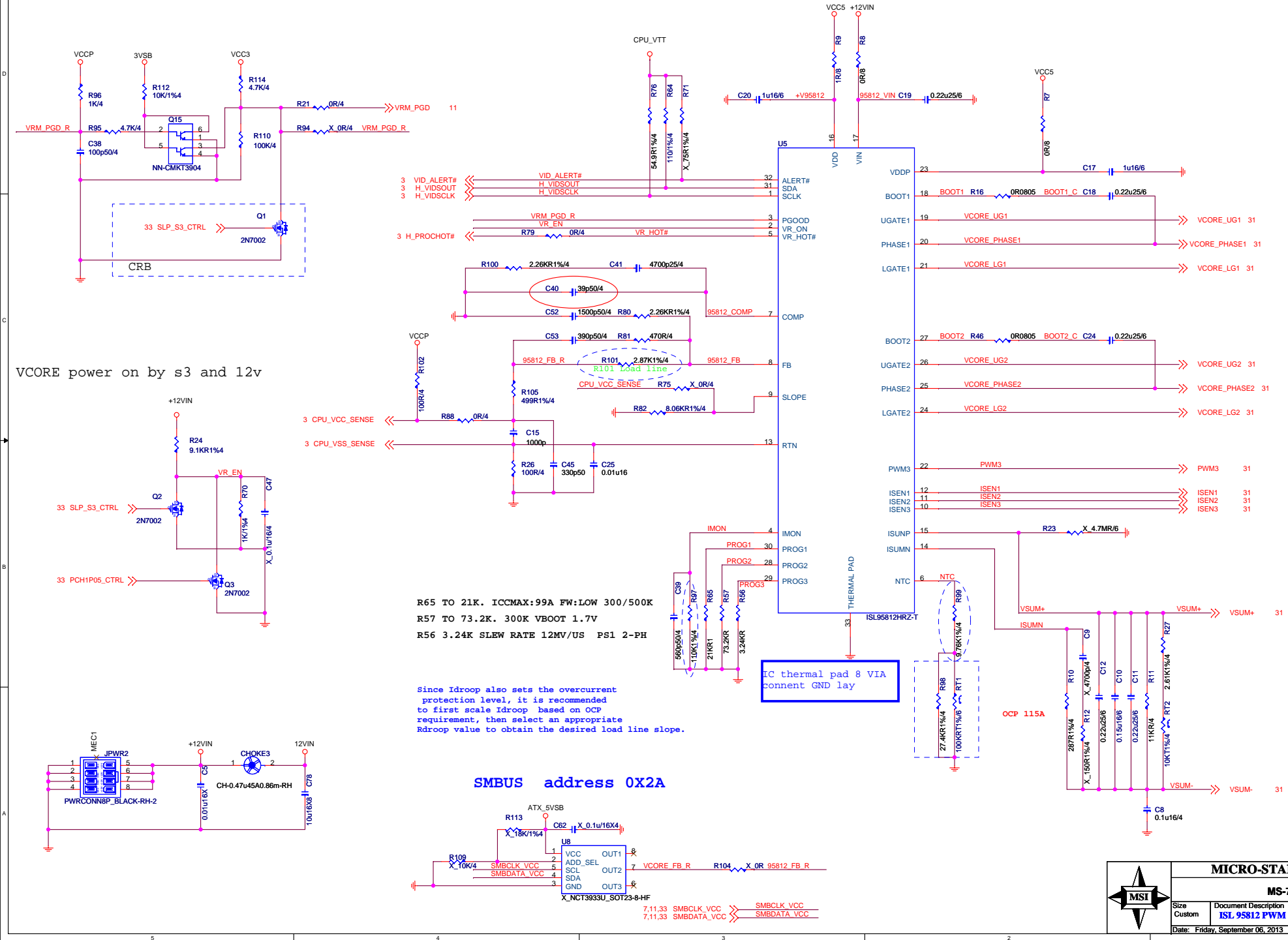
FRONT USB PORT 8,9

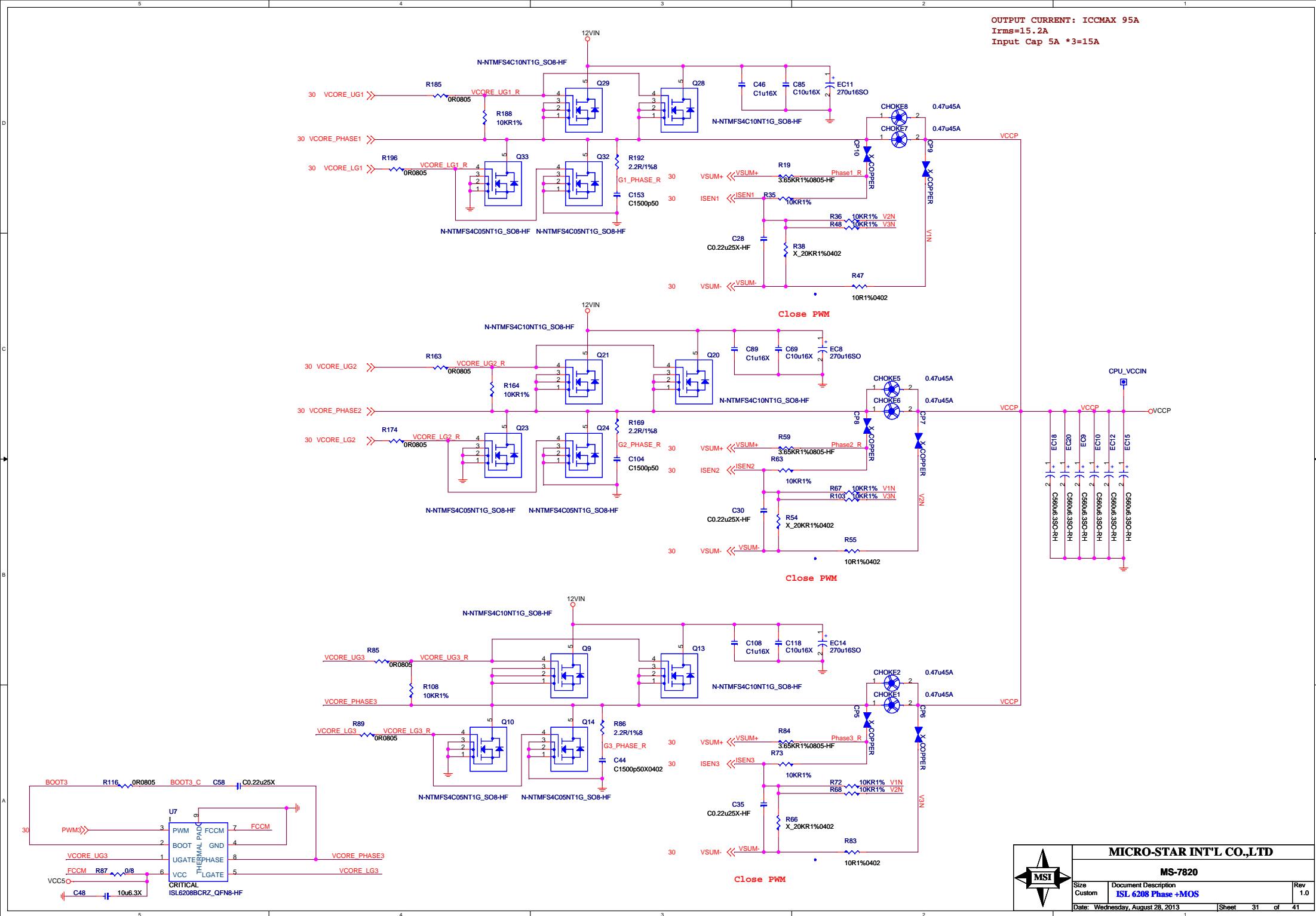


FRONT



Size Custom	Document Description Rear I/O & USB2.0 Connector	Rev 1.0
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DDR Power:1.5V

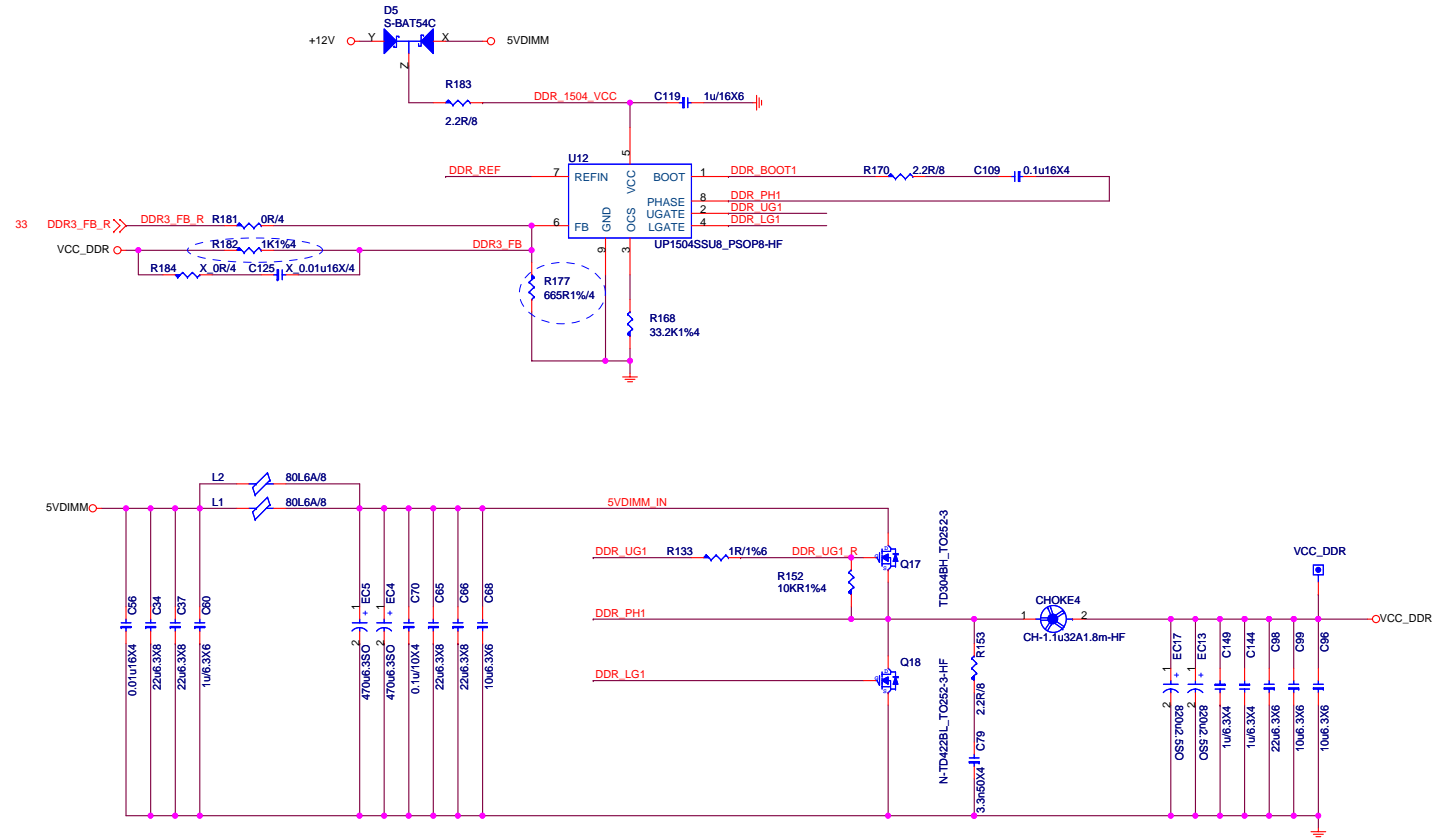
DDR3_1.5V 4.5A+6A+0.4A=15.9A

4.5A FOR CPU

6A FOR 2DIMM

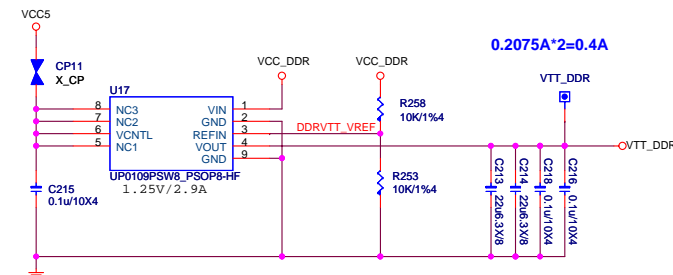
0.4A FOR DDR VTT

5A FOR DDR PCH



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



$$0.2075A \times 2 = 0.4A$$

P.S. Only for meet Intel power down sequence.

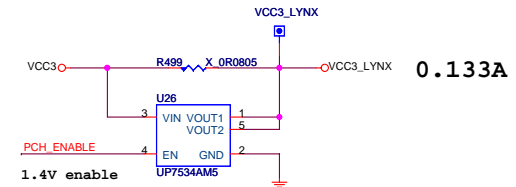
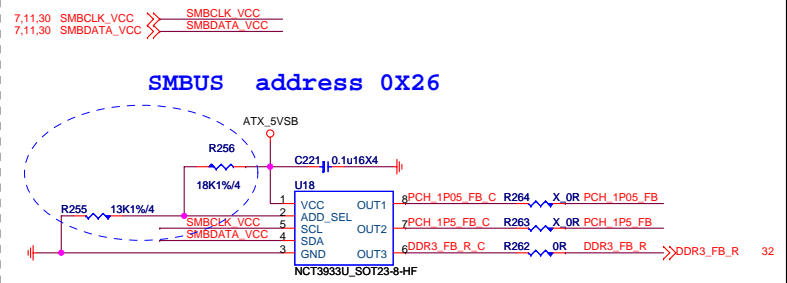
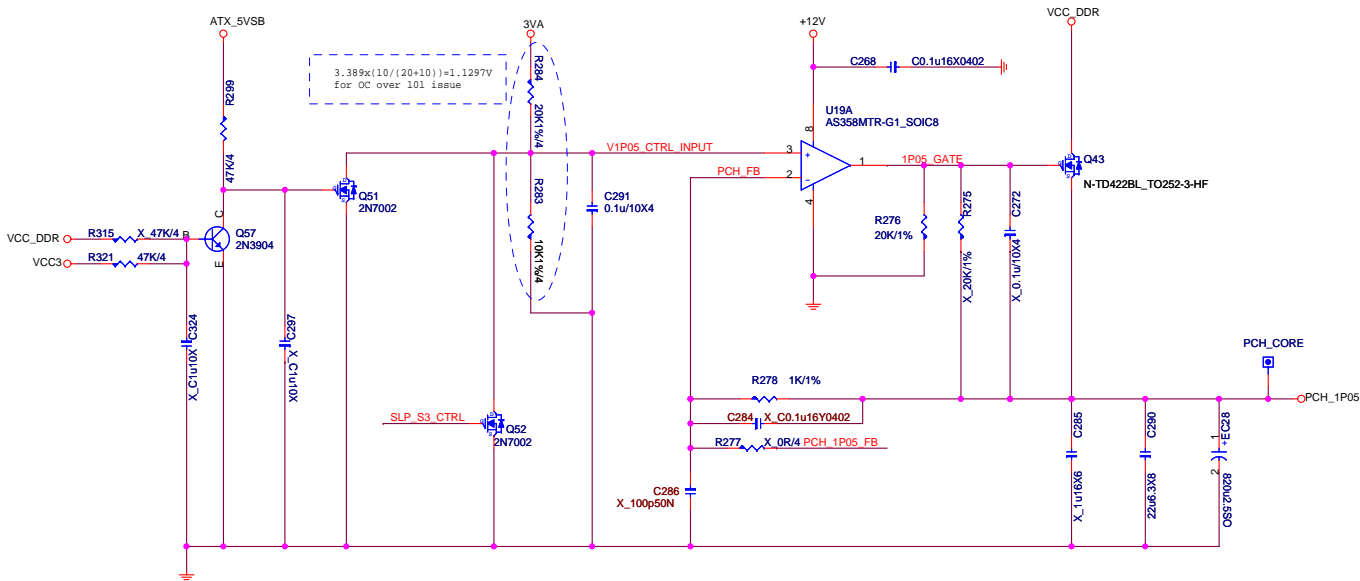


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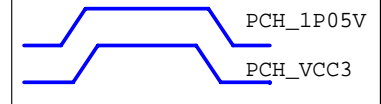
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Size	Document Description	Rev
Custom	DDR Power - UP1504S 1-Phase MOS	1.0
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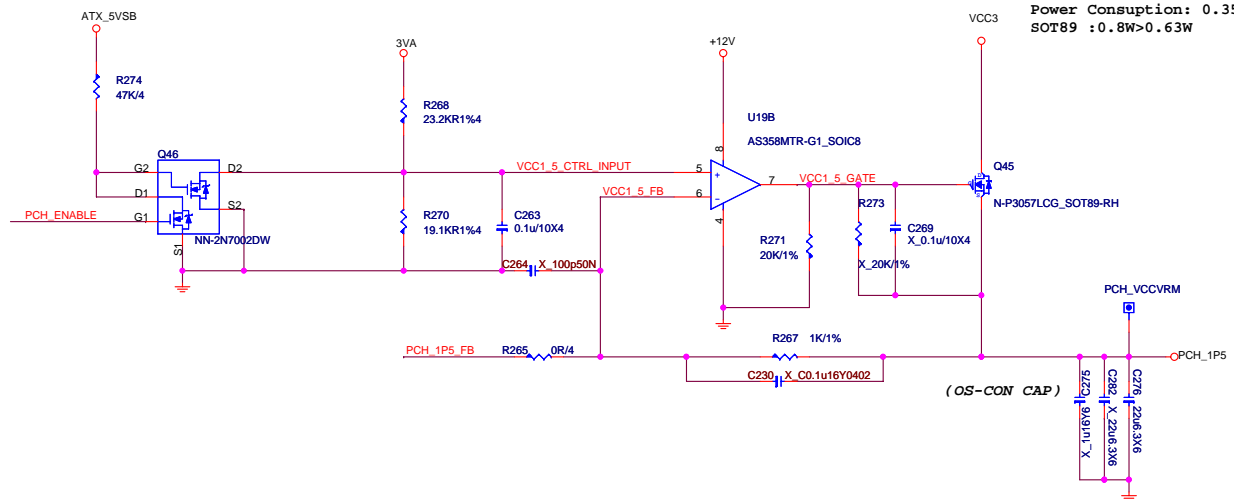
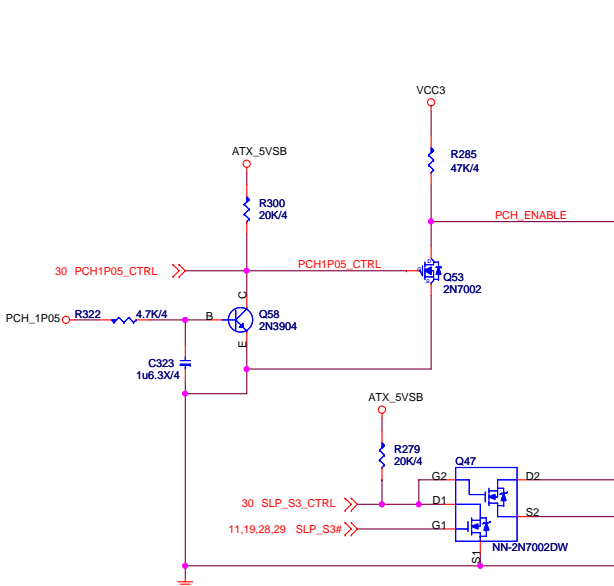
PCH Power:1.05V 5.747A



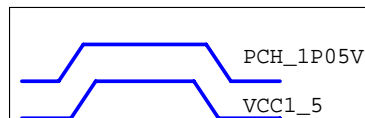
```
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH
```



PCH Power:1.5V 0.263A



```
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH
```



Power Consuption: $0.35A * (3.3-1.5)V = 0.63W$
SOT89 : $0.8W > 0.63W$



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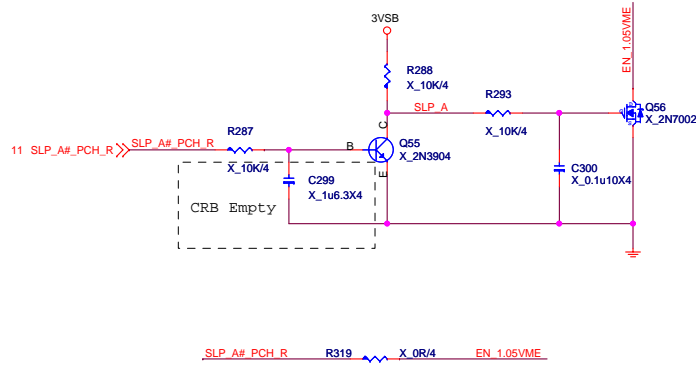
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Size	Document Description
Custom	PCH Power - OP+MOS

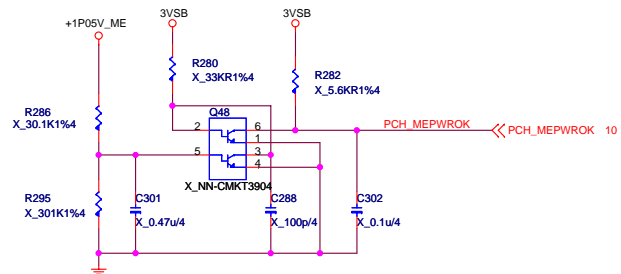
Rev	
1.0	

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SLP_A

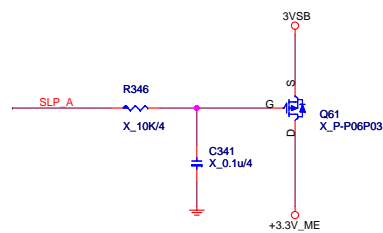


PCH_MEPWROK

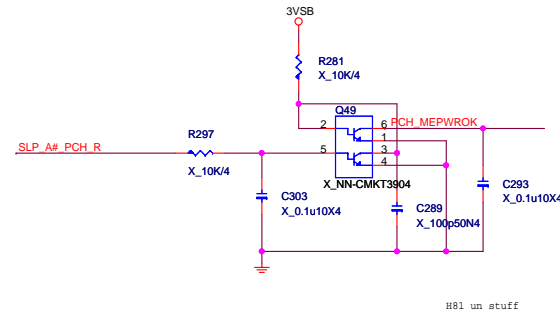
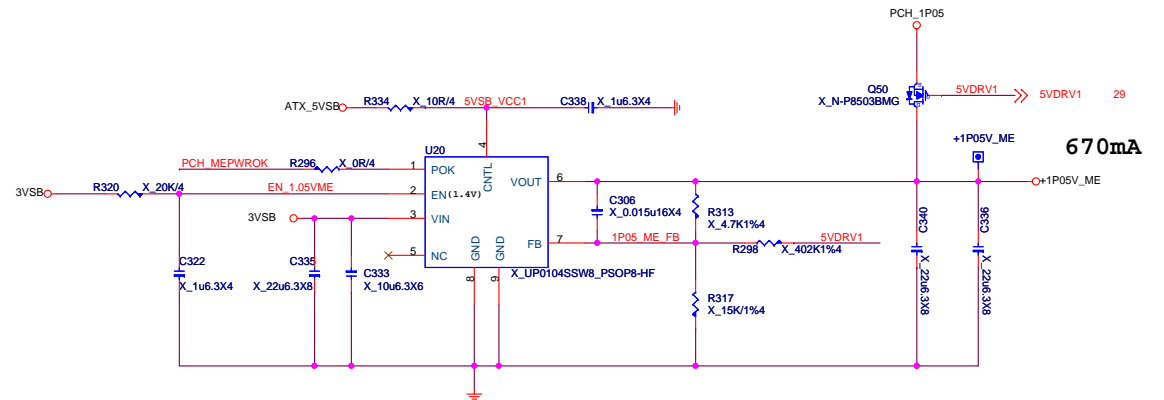


VccASW active to APWROK high 1ms

+3.3V_ME



+1.05V_ME(VCCIO_ME)



APWROK falling to VccASW falling 40ns

For INTEL ME BUG

B85->Stuff R412
H81->Stuff R407

VCC3 0R/4
+3.3V_ME 0R/4
CSPI_VCC3

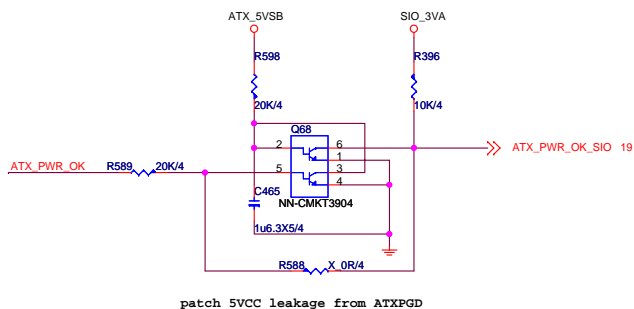
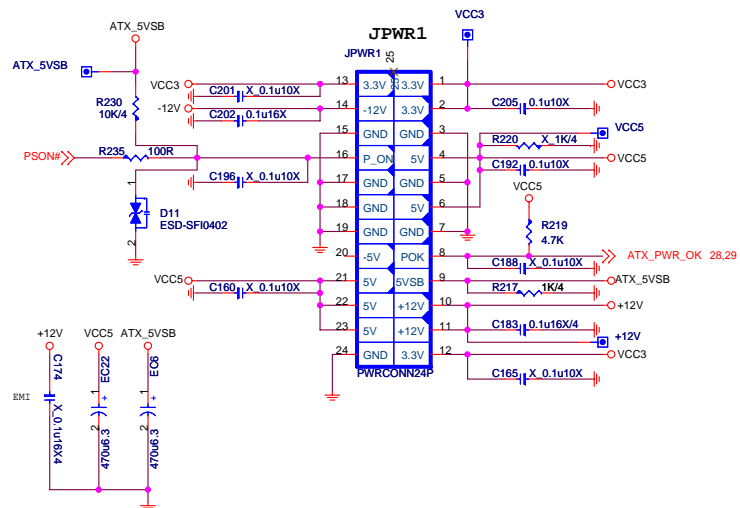


MICRO-STAR INT'L CO.,LTD

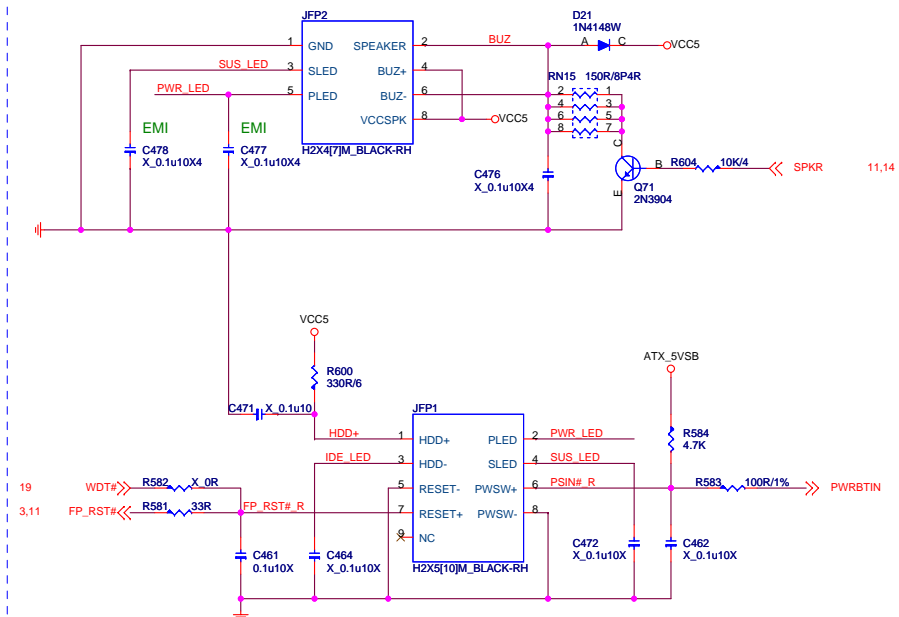
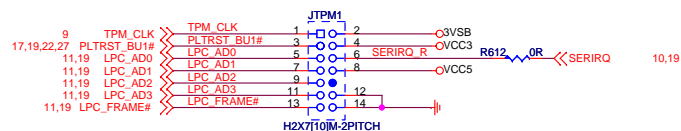
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Size	Document Description	Rev
Custom	ME POWER	1.0
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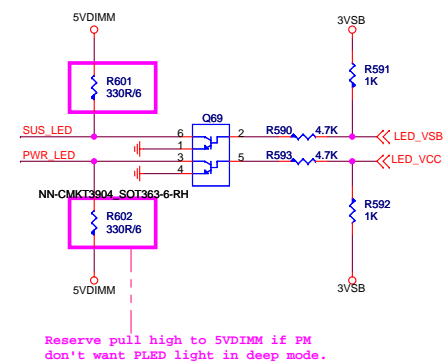
ATX POWER CONNECTOR



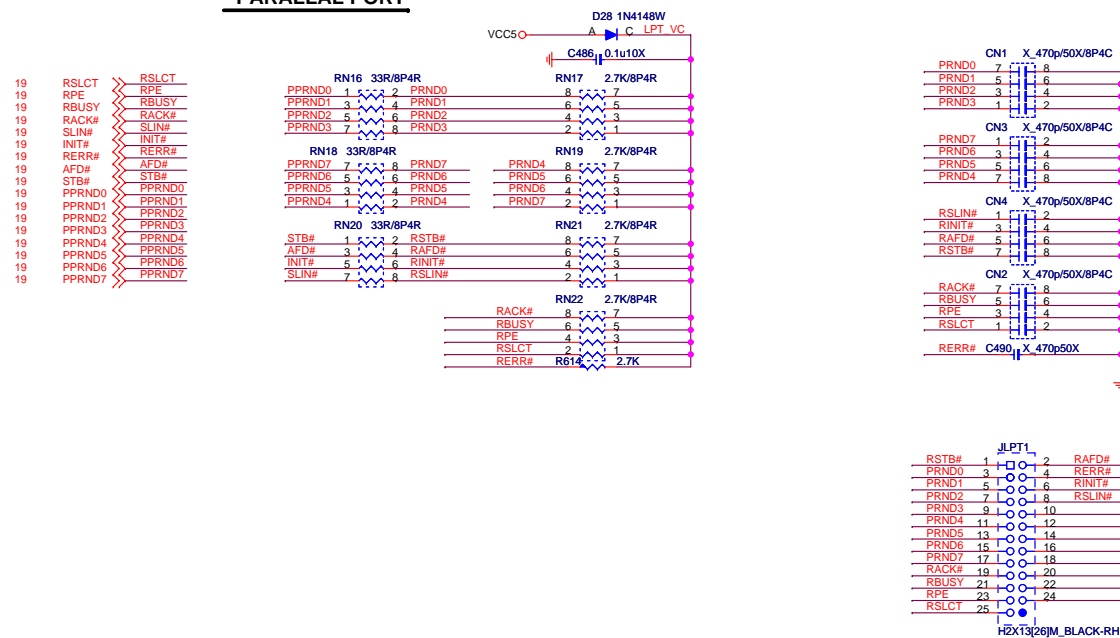
TPM



LED (for Fintek 71869)



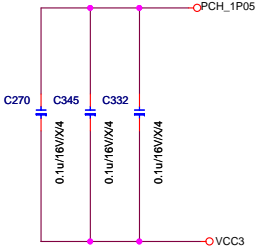
PARALLAL PORT



MICRO-STAR INT'L CO.,LTD

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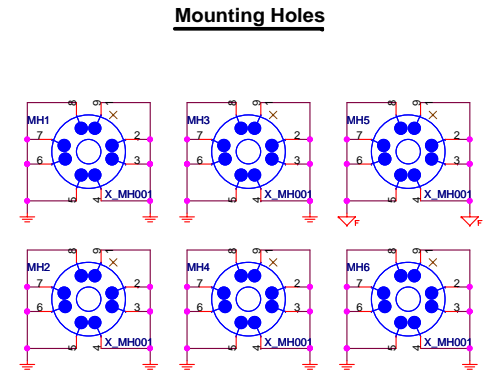
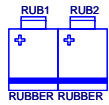
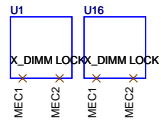
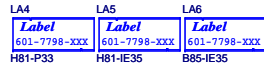
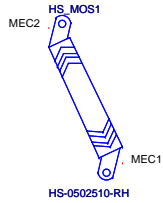
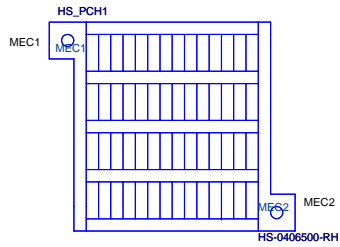
Size Custom	Document Description ATX F_Panel/EMI/TPM	Rev 1.0
Date: Wednesday, August 28, 2013		Sheet 35 of 41



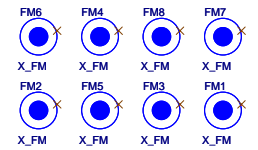
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Optical Fiducial Marks-120



Simulation

